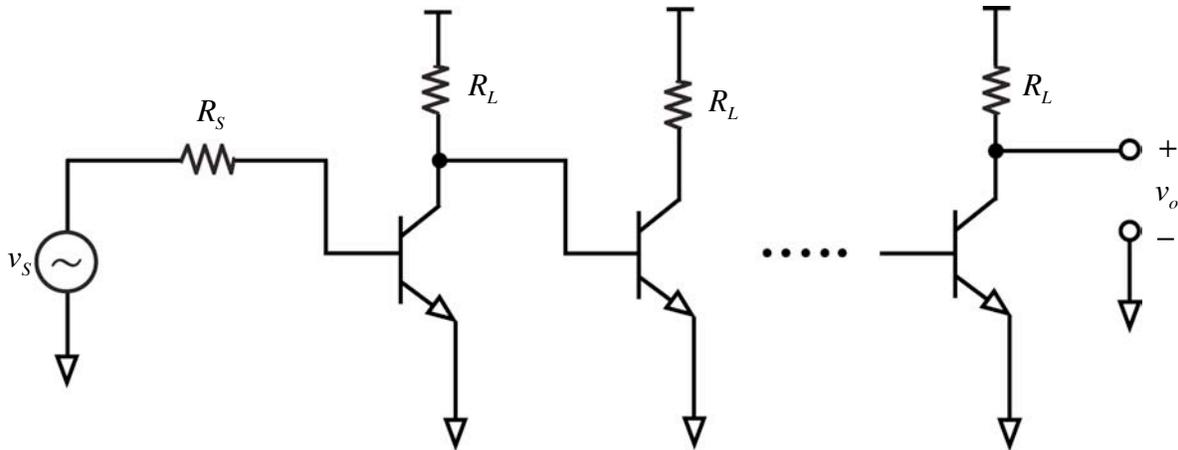


6.301 Solid State Circuits

Recitation 6: Bandwidth in Multistage Amplifiers

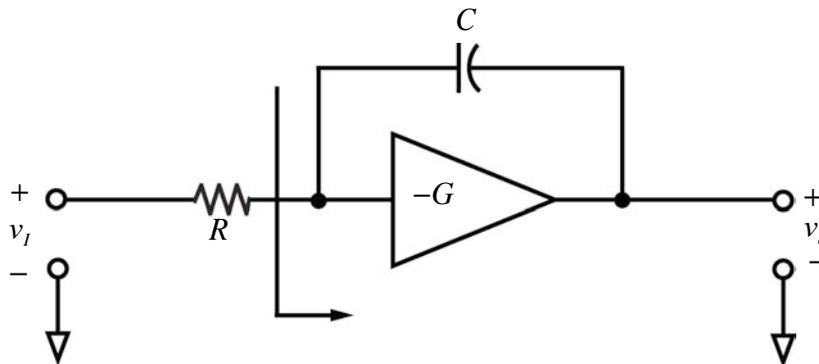
Prof. Joel L. Dawson

In the last recitation, we talked about “managing” the R s and C s, as well as the Miller Effect, to achieve high bandwidths. What I showed you were a couple of architectural tricks, namely the cascode and the architecture of the $\mu A733$, for getting high bandwidths. But it turns out that there are less glamorous ways of optimizing for bandwidth. Consider a cascade of common emitter stages:



The number of stages that we use to realize the desired gain is a choice that we can intelligently make. We'll start to see how in this recitation.

Let's start our investigation with the simple amplifier model shown below:

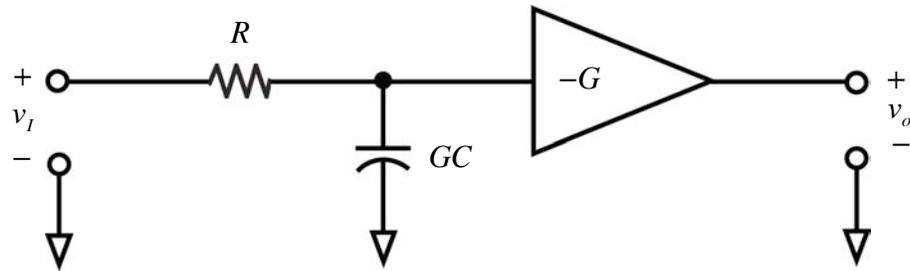


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Recitation 6: Bandwidth in Multistage Amplifiers

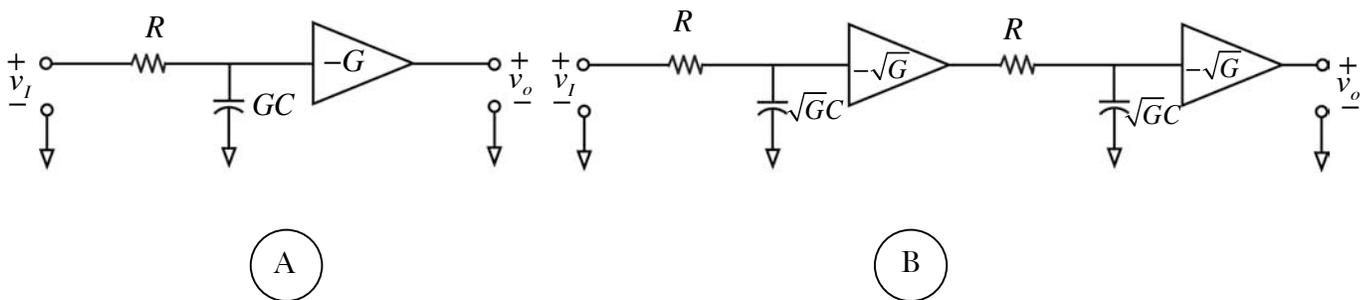
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Using our understanding of the Miller effect, we know that the input capacitance is going to be $(1+G)C \approx GC$. If the amplifier has zero output impedance, we can redraw this circuit as:



CLASS EXERCISE

Using the method of open circuit time constants, determine which topology has better (higher, in this case) bandwidth:



Assume $|G| \gg 1$.

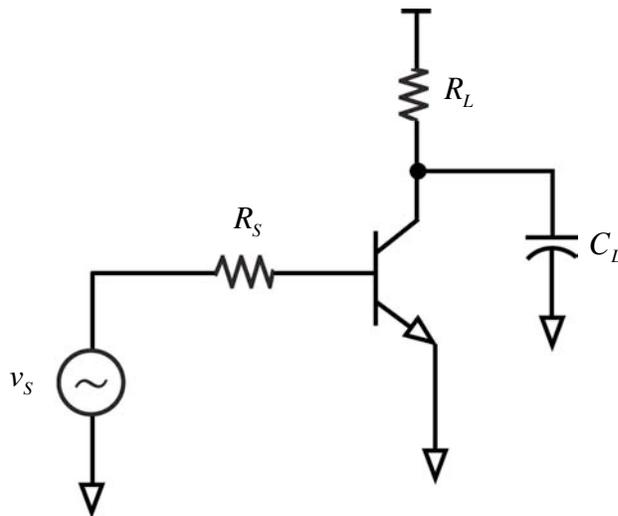
(Workspace)

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We see that even though the overall gain did not change, for large gains we do better by breaking the amplifier up into stages. This is our hint that choosing the number of stages is another way to manage our time constants.

Let's investigate this with real circuits now. We'll start with a single common-emitter stage.



$$I_C = 1\text{mA} \rightarrow g_m = 0.04\text{S}$$

$$r_\pi = 2.5\text{k}\Omega$$

$$r_b = 0$$

$$C_\pi = 20\text{pF}$$

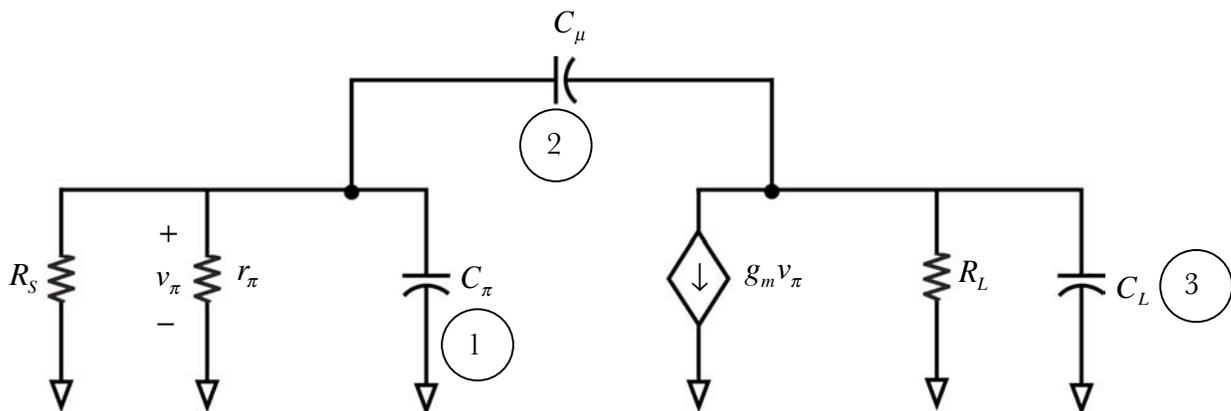
$$C_\mu = 2\text{pF}$$

$$R_s = 2.5\text{k}\Omega$$

$$R_L = 5\text{k}\Omega$$

$$C_L = 10\text{pF}$$

$$a_v = 100$$



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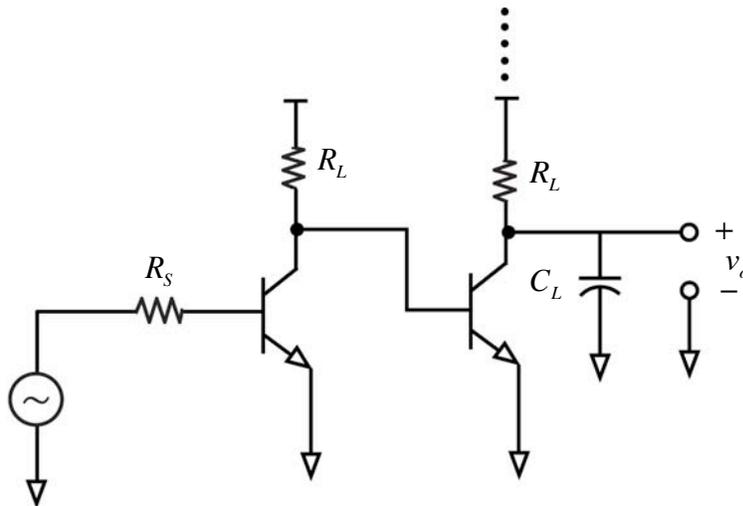
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Dutifully, we commit ourselves to the OCT calculation:

$$\begin{aligned}\tau_{10} &= C_{\pi} (R_s \parallel r_{\pi}) = (20 \text{ pF})(2.5 \text{ k}\Omega \parallel 2.5 \text{ k}\Omega) = 25 \text{ ns} \\ \tau_{20} &= C_{\mu} (\text{LEFT} + \text{RIGHT} + g_m \cdot \text{LEFT} \cdot \text{RIGHT}) \\ &= C_{\mu} (R_s \parallel r_{\pi} + R_L + g_m (R_s \parallel r_{\pi}) R_L) \\ &= 2 \text{ pF} (2.5 \text{ k}\Omega \parallel 2.5 \text{ k}\Omega + 5 \text{ k}\Omega + (0.04 \text{ V}) (2.5 \text{ k}\Omega \parallel 2.5 \text{ k}\Omega) 5 \text{ k}\Omega) \\ &= 513 \text{ ns} \\ \tau_{30} &= C_L R_L = 10 \text{ pF} (5 \text{ k}\Omega) = 50 \text{ ns}\end{aligned}$$

$$\boxed{\Sigma \tau = 588 \text{ ns} \rightarrow f_h = 270 \text{ kHz}}$$

This is all in the notes. Now we're going to look at two stages with equal R_L :



But here we're going to do something a little different. We're going to require that the overall gain remain the same, of course. But we're now going to go the extra step and keep the power dissipation the same. That is, each transistor will now be running at $500 \mu\text{A}$ instead of 1 mA . We expect an amplifier that consumes twice as much power to have superior performance. The measure of a topology is whether or not it gives better performance for the same amount of power.

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For each transistor now, our small-signal parameters have changed:

$$I_C = 500\mu A \rightarrow g_m = \frac{qI_C}{kT} = \frac{500\mu A}{25mV} = 0.02\mathfrak{U}$$

$$r_\pi = \frac{\beta}{g_m} = 2 \cdot 2.5k\Omega = 5.0k\Omega$$

$$r_b = 0$$

$$C_\pi \approx C_b = g_m \tau_F = \frac{1}{2}(20pF) = 10pF$$

$$C_\mu = 2pF, R_s = 2.5k\Omega, C_L = 10pF$$

What do we use for R_L ? We require

$$a_v = \left(\frac{r_\pi}{R_s + r_\pi} \right) g_m (R_L \parallel r_\pi) g_m R_L = 100$$

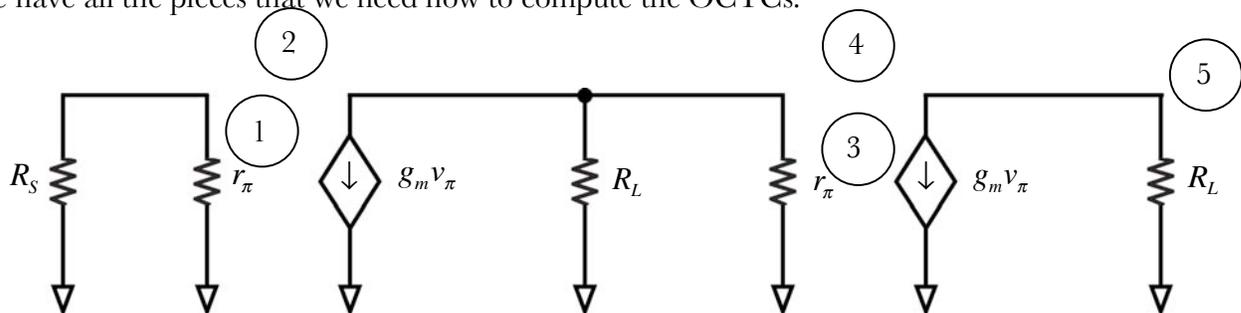
$$\left(\frac{5.0k\Omega}{2.5k\Omega + 5k\Omega} \right) (0.02\mathfrak{U}) \left(\frac{R_L \cdot 5.0k\Omega}{R_L + 5.0k\Omega} \right) (0.02\mathfrak{U}) R_L = 100$$

$$\frac{R_L^2 \cdot 5.0k\Omega}{R_L + 5.0k\Omega} = 3.75 \times 10^5 r^2$$

$$R_L^2 - 75R_L - 3.75 \times 10^5 = 0$$

$$\boxed{R_L = 650\Omega}$$

We have all the pieces that we need now to compute the OCTCs.



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$$\tau_{10} = C_{\pi} (R_s \parallel r_{\pi}) = 10 \text{ pF} (2.5 \text{ k}\Omega \parallel 5 \text{ k}\Omega) = 17 \text{ nS}$$

$$\begin{aligned} \tau_{20} &= C_{\mu} (R_s \parallel r_{\pi} + R_L \parallel r_{\pi} + g_m (R_s \parallel r_{\pi}) (R_C \parallel r_{\pi})) \\ &= 2 \text{ pF} (1.7 \text{ k}\Omega + 575 \Omega + (0.02 \text{ V}) (1.7 \text{ k}\Omega) (575 \Omega)) = 44 \text{ nS} \end{aligned}$$

$$\tau_{30} = C_{\pi} (R_L \parallel r_{\pi}) = 10 \text{ pF} (575 \Omega) = 5.8 \text{ nS}$$

$$\begin{aligned} \tau_{40} &= C_{\mu} (R_L \parallel r_{\pi} + R_L + g_m (R_L \parallel r_{\pi}) R_L) \\ &= 2 \text{ pF} (575 \Omega + 650 \Omega + (0.02 \text{ V}) (575 \Omega) (650 \Omega)) = 17.4 \text{ nS} \end{aligned}$$

$$\tau_{50} = C_L R_L = (10 \text{ pF}) (650 \Omega) = 6.5 \text{ nS}$$

$\Sigma \tau = 90.7 \text{ nS} \Rightarrow f_h = \frac{1}{2\pi(90.7 \text{ nS})} = 1.8 \text{ MHz}$

(Compare this with Dr. Lundberg's notes, where we get a final answer of 1.9MHz.)

What just happened here? We started with a single common emitter stage, aimed for a gain of 100, and got a bandwidth of 270kHz. By adding a second stage, but without increasing the power dissipation, we wound up with an almost $7 \times$ bandwidth improvement!

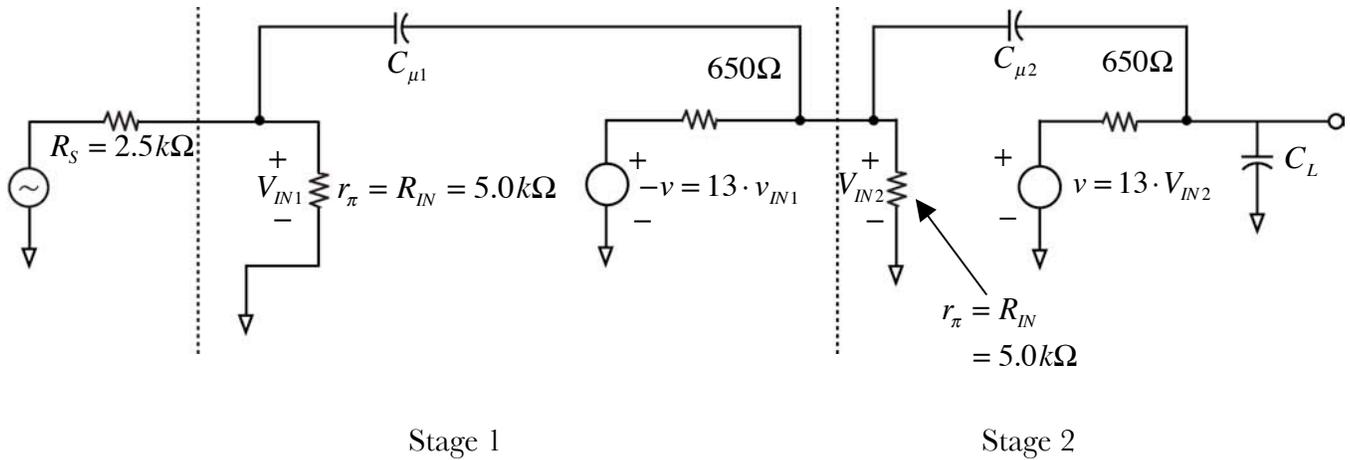
Power-constrained optimization of circuits has been one of the dominant themes in circuit research and development. I have even heard of one engineer who spoke of designing for low-power as a "way of life." It is interesting to ask yourself how to get a task done while expanding the minimum possible energy...

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Before we leave the cascade, there's at least one more degree of freedom to explore: Mismatching the R_L s. Right now, our 2-port view of the world looks something like:



We can see that we've set up the two stages for equal gains, even though the first stage sees a much worse source impedance than the second. It turns out to be smarter to shift more gain to the second stage, and correspondingly reduce the first stage gain.

These are the kinds of games that designers must sometimes play...

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