

Reading...

- Horowitz and Hill
 - Finish Chapter 1, read Chapters 4&5
- Fraden
 - Interface Electronic Circuits Chapter (Chapter 4 of second edition)

Reactive Impedance

- The Capacitor 
 - Adds in parallel like resistors add in series
 - Reciprocal-adds in series like resistors add in parallel
- Impedance of capacitor = $-j/\omega C = -j/(2\pi fC)$
 - Pass AC, block DC
 - Capacitor current: $I_c = CdV/dt$
- Impedance of inductor = $j\omega L = j(2\pi fL)$
 - Block AC, pass DC
 - Inductor Voltage: $V = LdI/dt$



Passive RC Filters

- Passive LP Filter: RC network: $f_c = 1/(2\pi RC)$

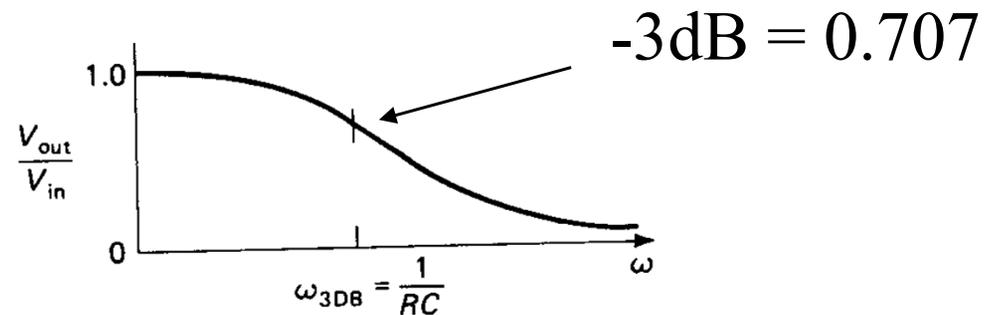
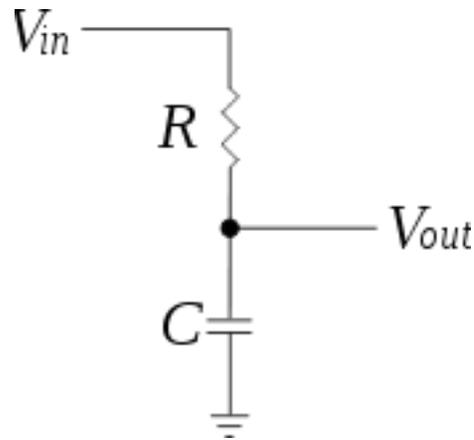


Figure 1.59. Frequency response of low-pass filter.

This image is public domain.

© Cambridge University Press. All rights reserved. This content is excluded from our Creative Commons license. For more information, see <http://ocw.mit.edu/fairuse>.

- Passive HP filter: RC network: $f_c = 1/(2\pi RC)$

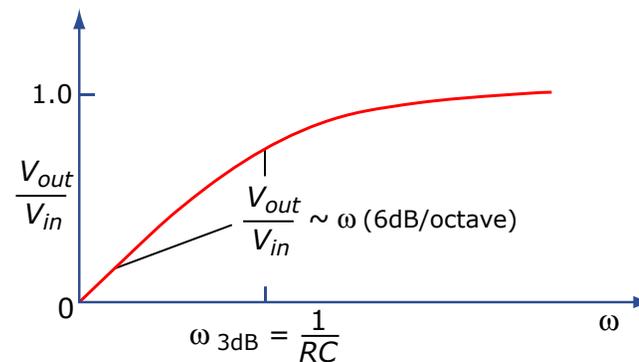
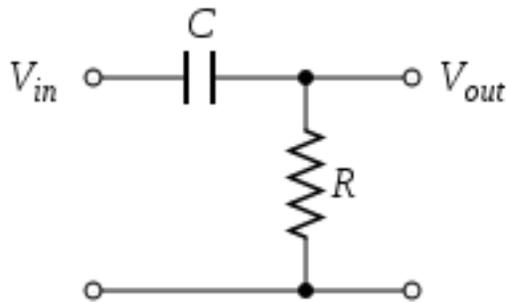


Image by MIT OpenCourseWare.

Frequency response of a high-pass filter.

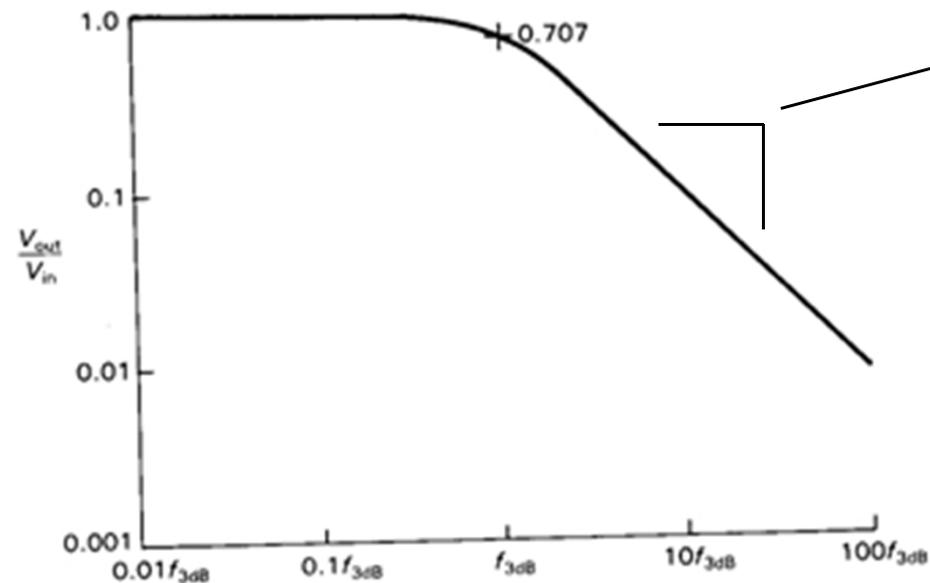
This image is public domain.

Passive RC Filter Rolloff

Bode Plot:

Freq. Response as a log-log plot

The rest of this figure has been removed due to copyright restrictions. It can be viewed on page 38 of *The Art of Electronics*, P. Horowitz and W. Hill. See: page 38 of *The Art of Electronics* on [Google Books](#).

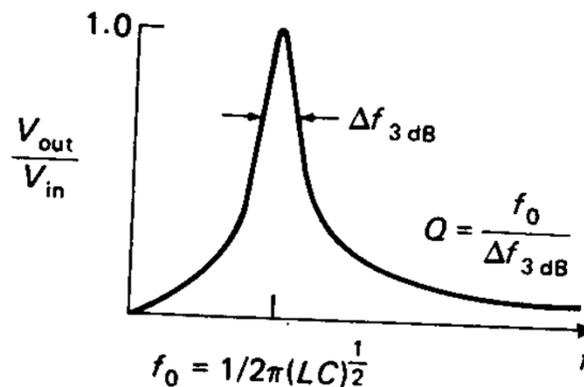
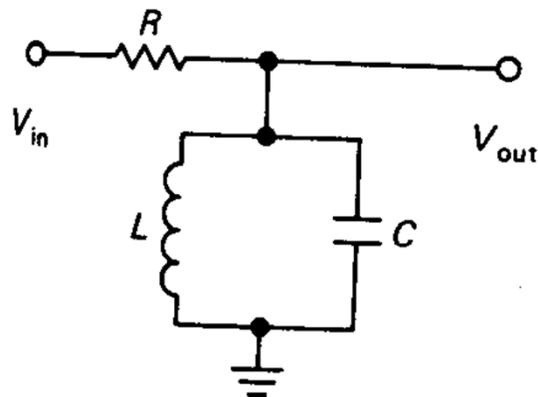


Rolloff is 6 dB per Octave (2x)
20 dB per Decade (10x)

© Cambridge University Press. All rights reserved. This content is excluded from our Creative Commons license. For more information, see <http://ocw.mit.edu/fairuse>.

Passive RLC Filters

- Resonant parallel RLC bandpass filters

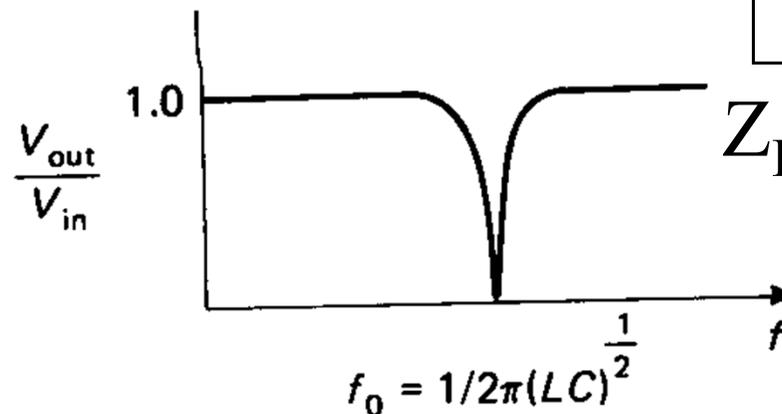
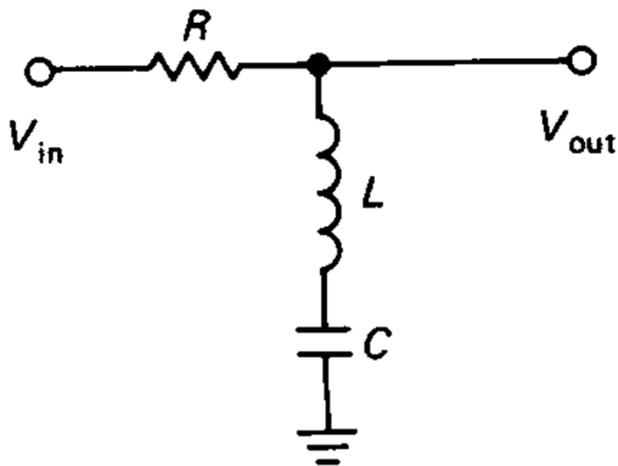


$$Q = \omega_0 RC$$

$$= f_0 / \Delta f_{3\text{dB}}$$

$$Z_{LC} \rightarrow \infty @ f_0$$

- Resonant series RLC notch filters



$$Q = \omega_0 (L/R)$$

$$= f_0 / \Delta f_{3\text{dB}}$$

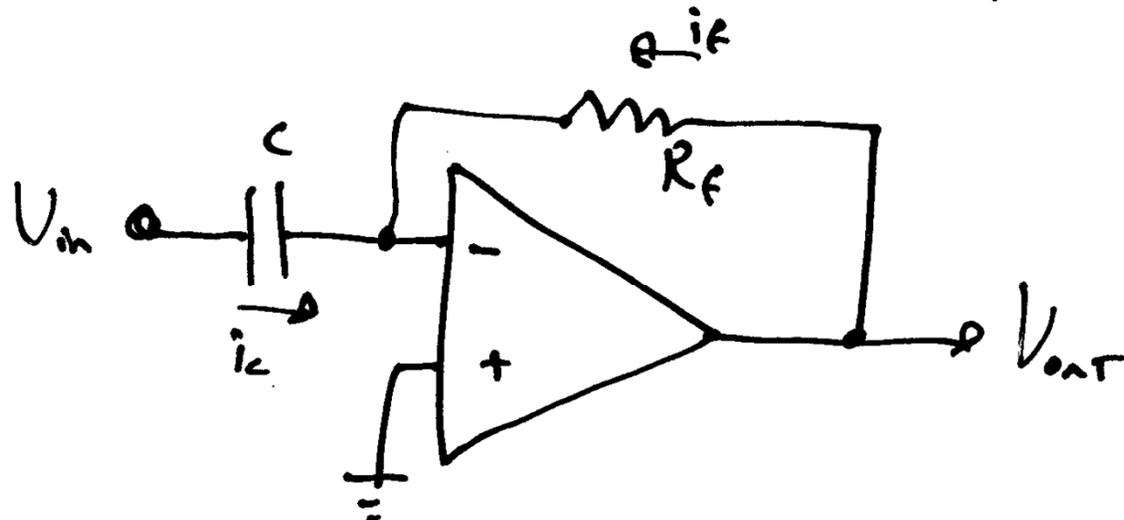
$$Z_{LC} \rightarrow 0 @ f_0$$

Active Filters

- The Differentiator
- The Active High-Pass Filter
- Principle of Feedback Inversion
- The Integrator
- The Leaky Integrator (LP filter)
- Buffered Passive Second-Order Filter
- Sallen-Key (or VCVS) LP, HP, BP filters
- Single-OpAmp VCVS BP filter

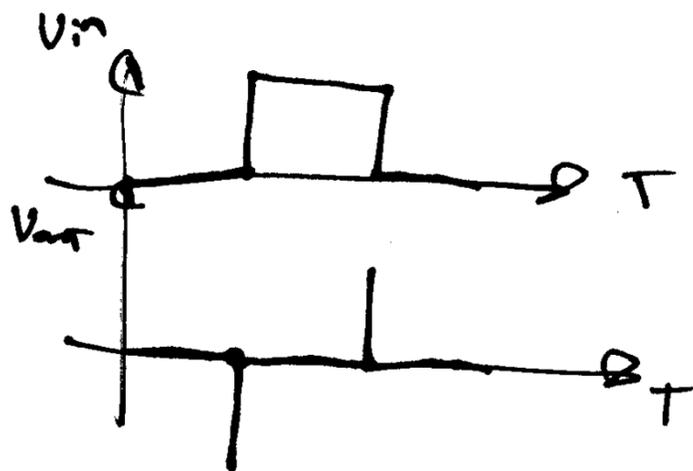
The Differentiator

The Differentiator



$$i_f = -i_c$$

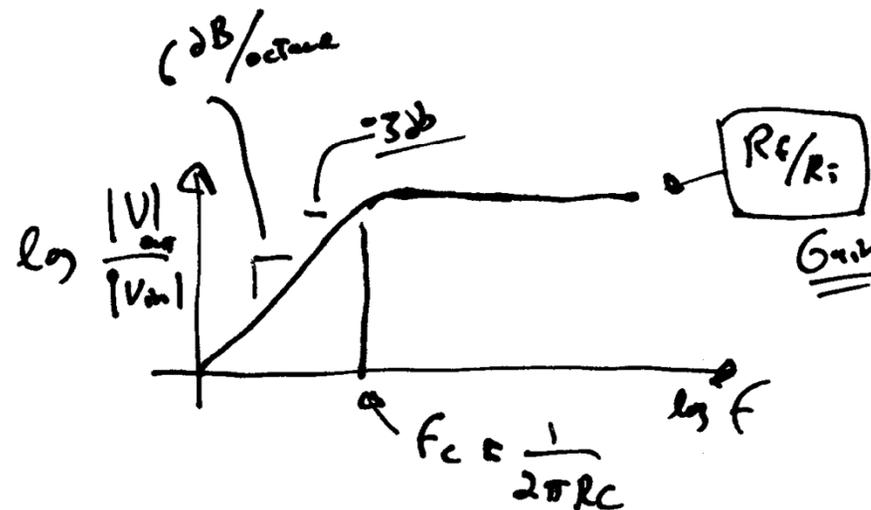
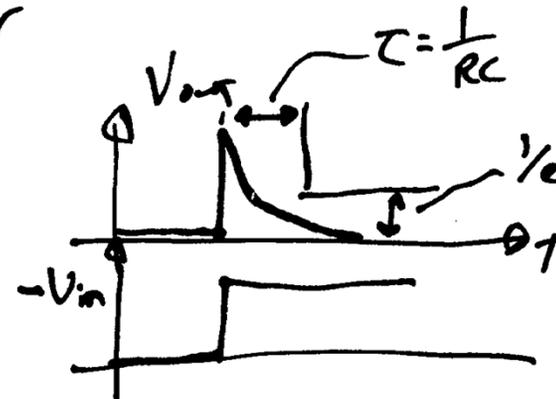
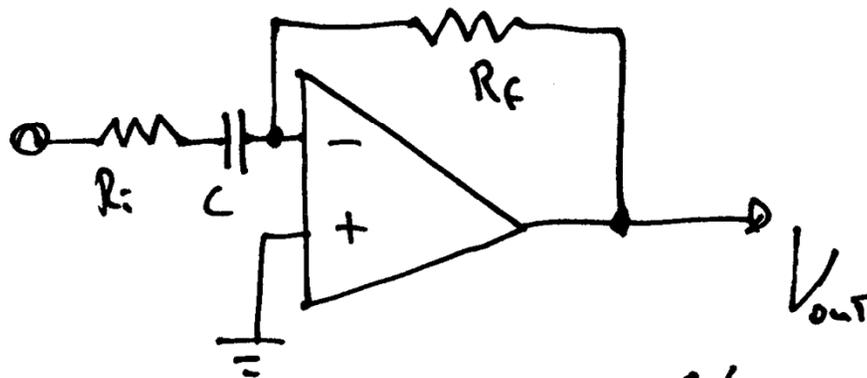
$$\frac{V_{OUT}}{R_f} = -C \frac{dV_{in}}{dT}$$



$$V_{OUT} = -R_f C \frac{dV_{in}}{dT}$$

The First-Order Active High Pass Filter

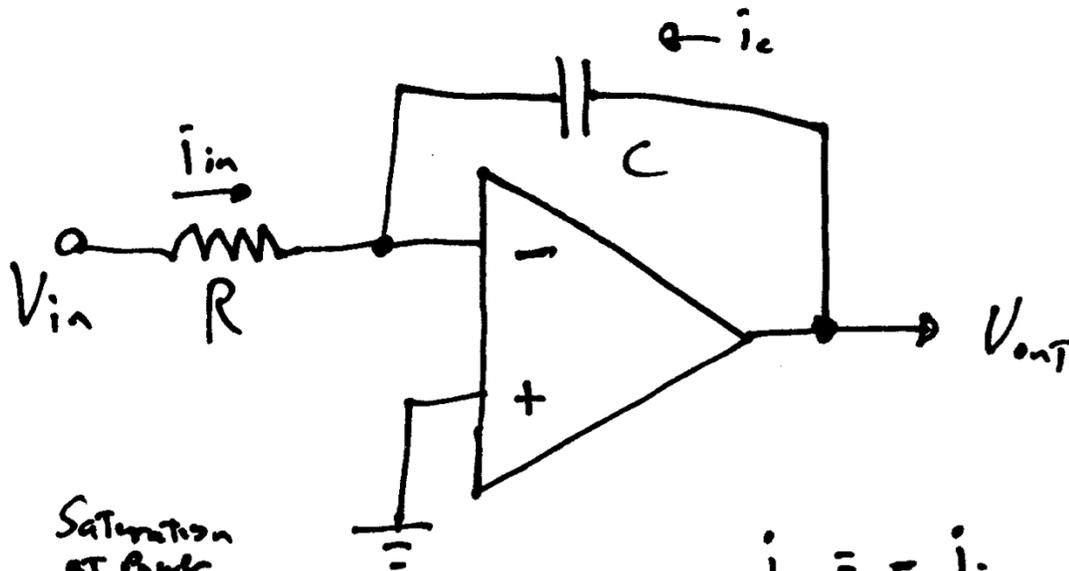
High Pass Filter



- Low impedance drive
- Voltage gain via R_f/R_i

The Integrator

The Integrator

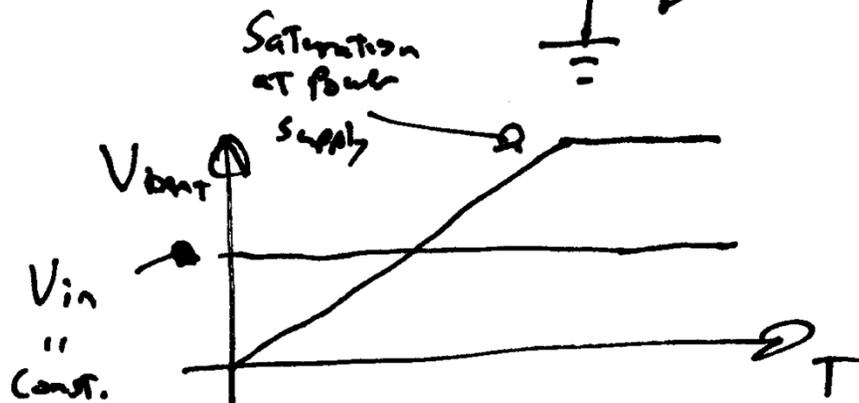


$$Z_c = \frac{1}{j\omega c}$$

$$i_c = C \frac{dV}{dT}$$

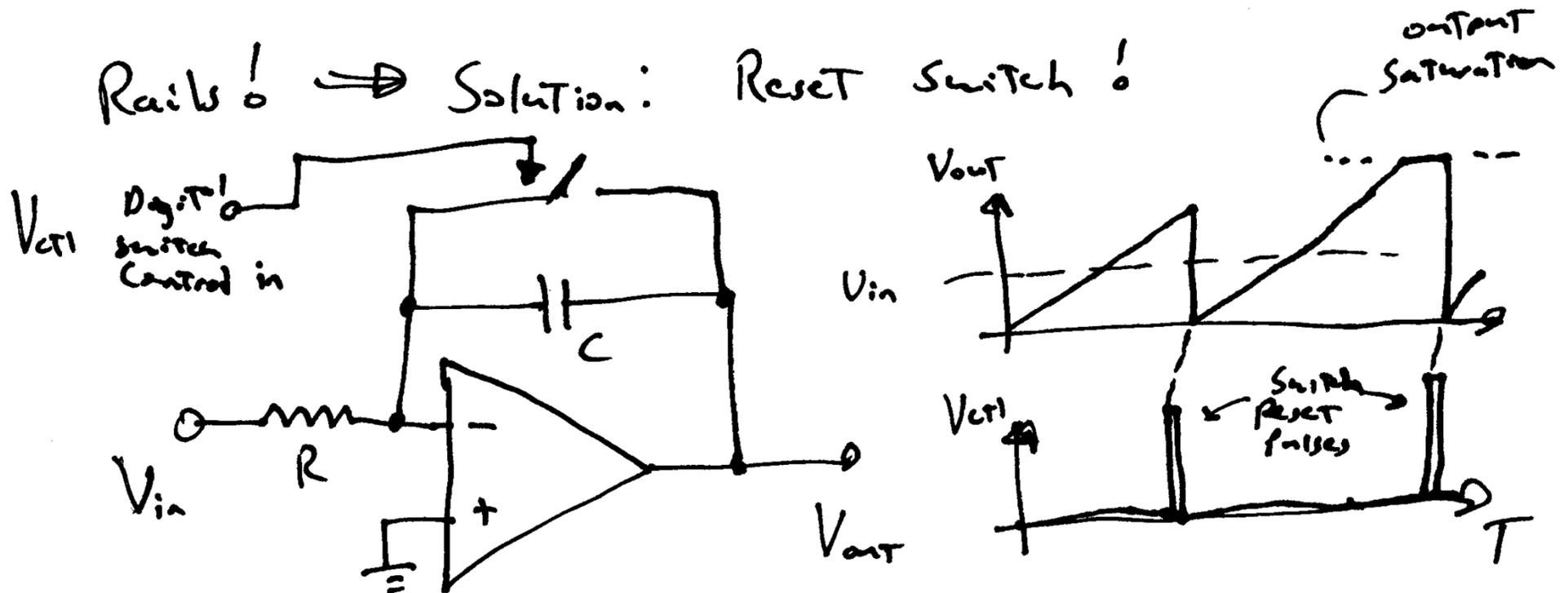
$$i_c = -i_{in} \Rightarrow C \frac{dV_{out}}{dT} = -\frac{V_{in}}{R}$$

$$\frac{dV_{out}}{dT} = -\frac{V_{in}}{RC} \Rightarrow \underline{\underline{V_{out} = -\frac{1}{RC} \int V_{in} dt}}$$



Saturates at rail!!

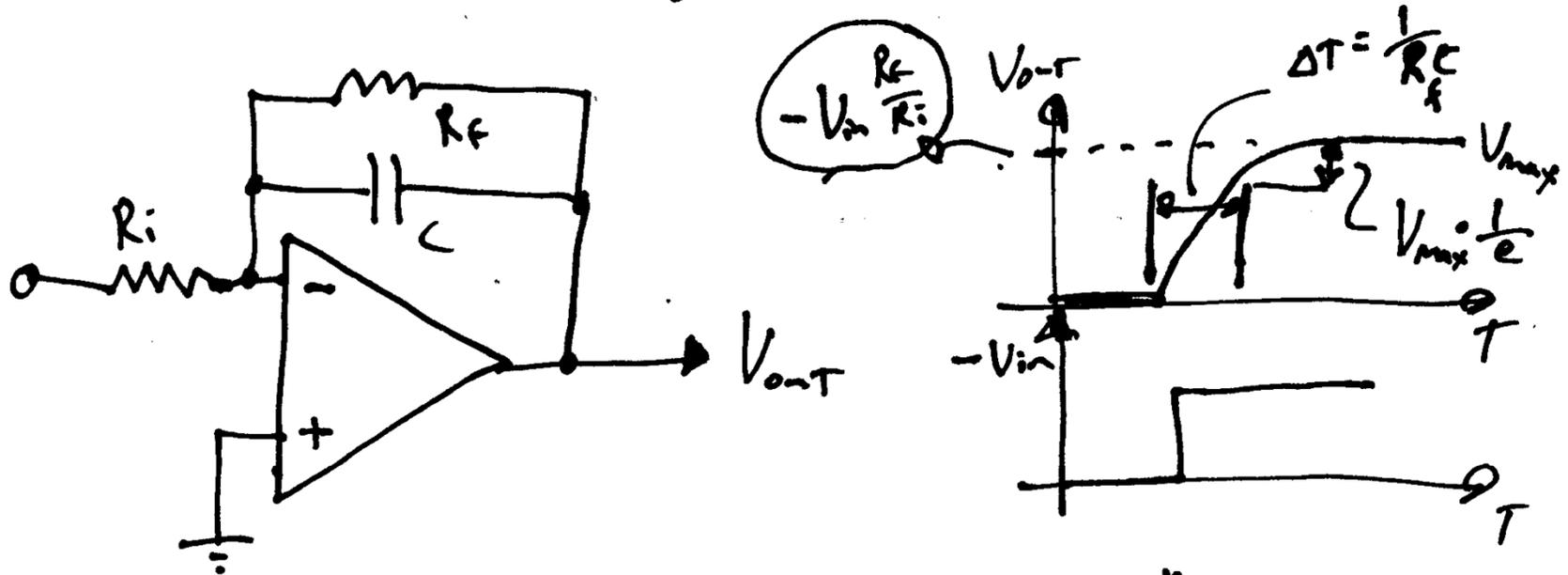
Integrator with Reset Switch



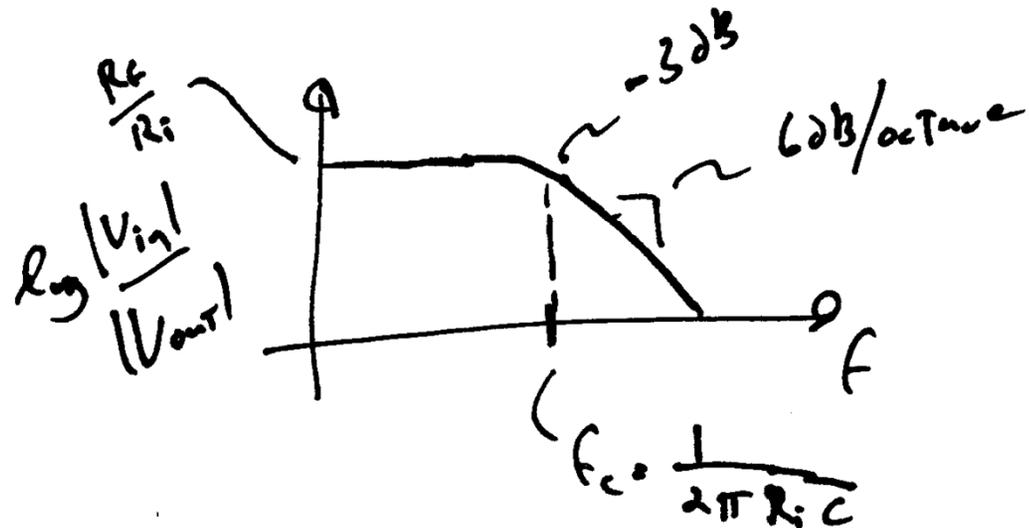
- Electronic switch in feedback forces output to ground when closed
 - Discharges capacitor
 - Resets Integrator!

The First-Order Active Low Pass Filter

The Leaky Integrator \rightarrow Low Pass Filter

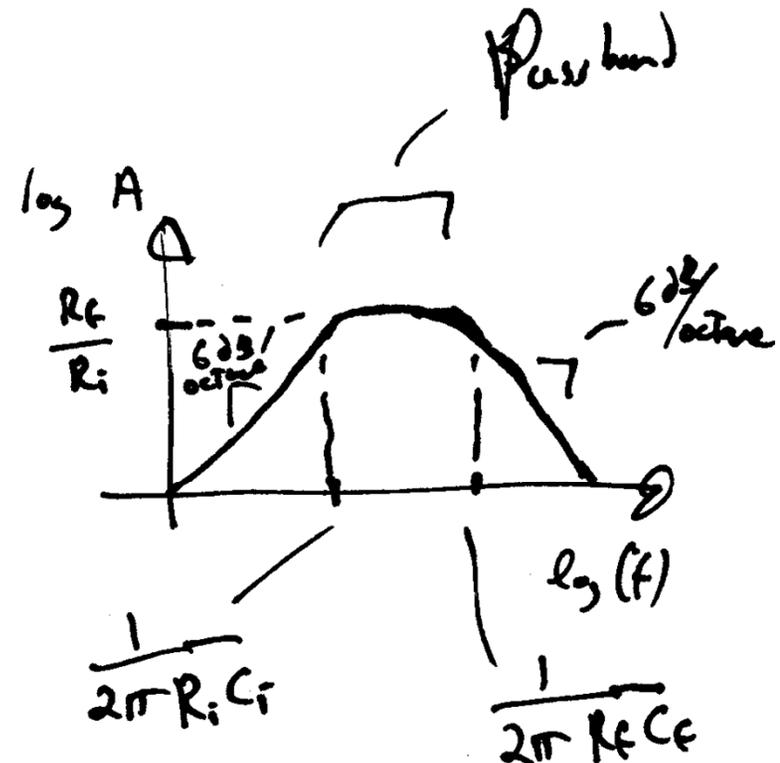
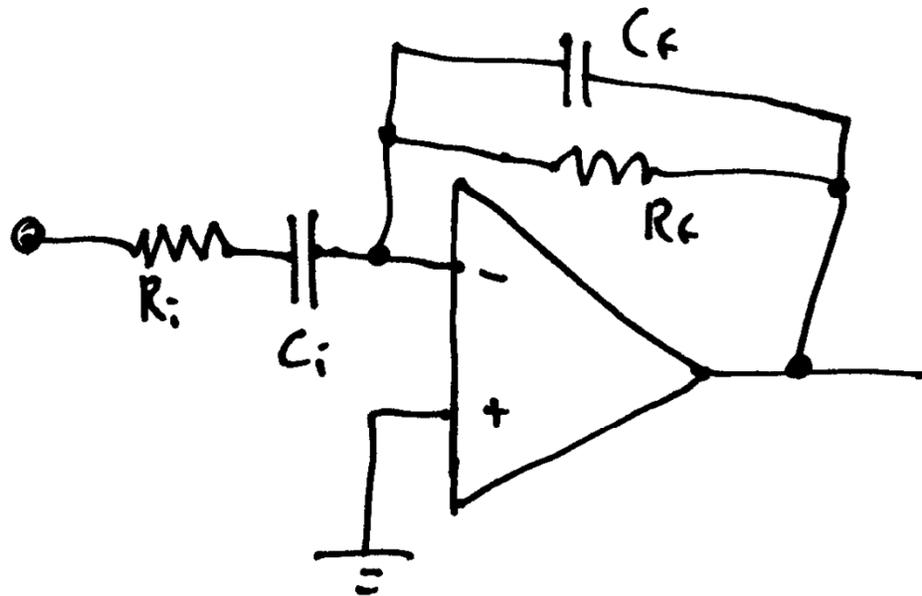


Low impedance
output !!
Voltage gain !!



The Band-Select Filter

Band - Select Filters



- Cascaded high and low pass filters
 - Always follow high-pass with low-pass (noise)
 - Low-Pass cutoff needs to be below high-pass cutoff!
 - No Q, first-order rolloffs

Modulars are Analog Computers?

Photo of a Compumedic Analog Computer from 1971 removed due to copyright restrictions. See: Old-Computers.com Museum.

Compumedic Analog Computer from 1971

Limitations on Filter Performance

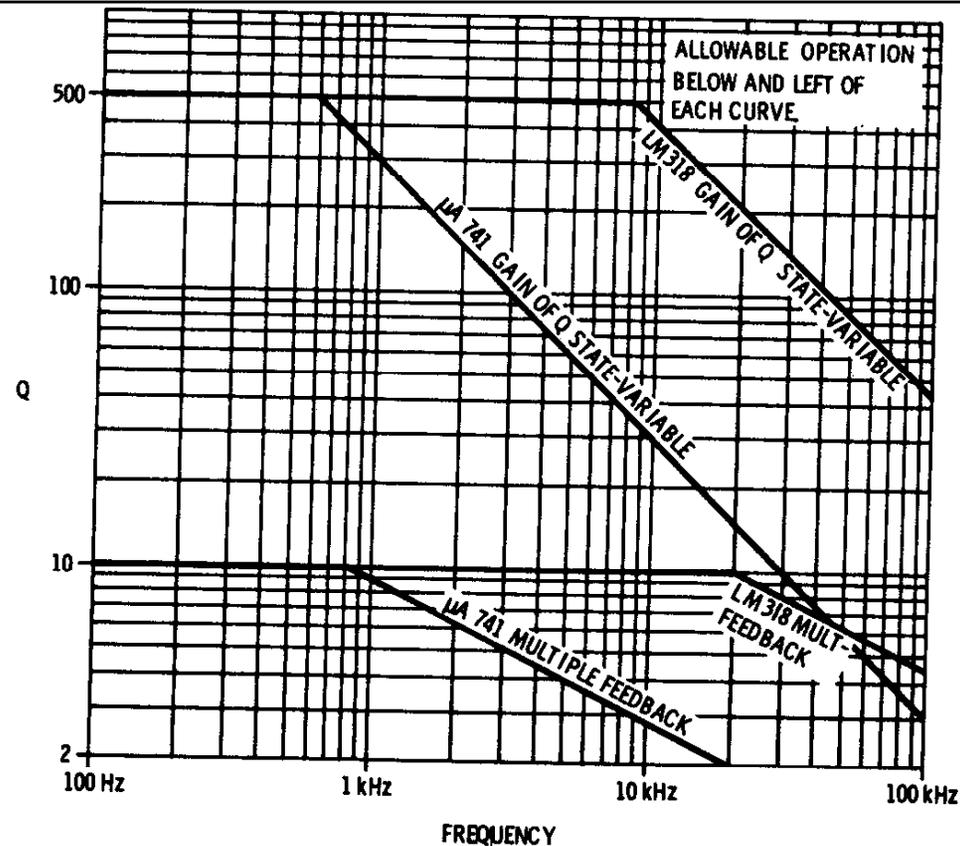


Fig. 7-14. Q and frequency limits for active bandpass filters, small output swings.

© Elsevier. All rights reserved. This content is excluded from our Creative Commons license. For more information, see <http://ocw.mit.edu/fairuse>.

- The choice of OpAmp affects how well a given filter will perform
 - Multiple-OpAmp filters can attain higher Q's than single-OpAmp filters
 - Faster OpAmp's work better too
 - Accumulated Phase Shifts can cause oscillation!

Voltage-Controlled Filter

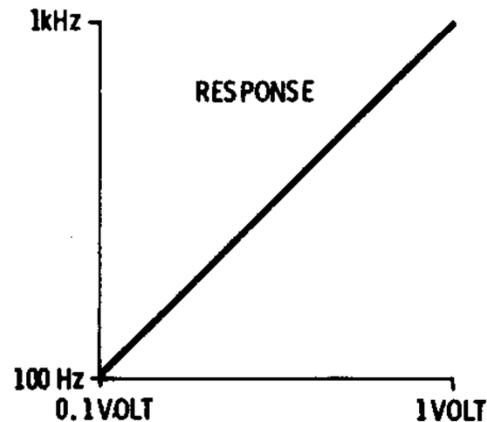
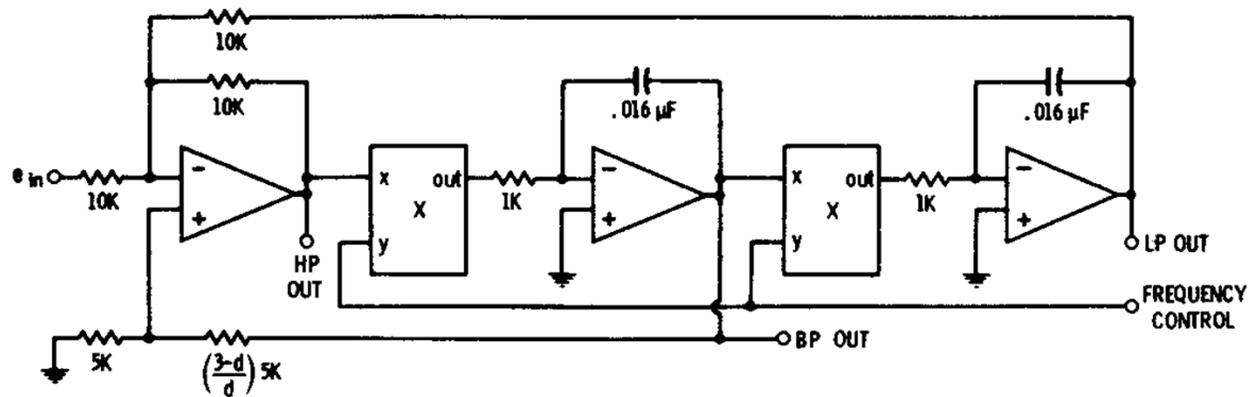


Fig. 9-5. Voltage-controlled filter using IC four-quadrant multipliers.

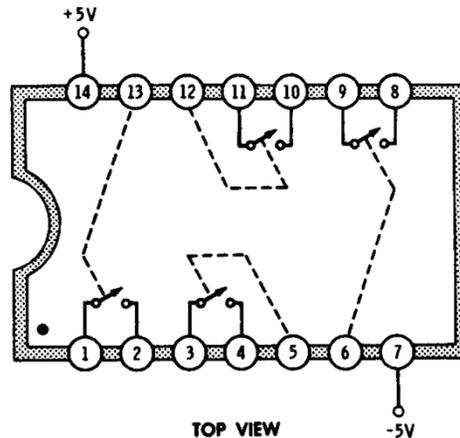
© Elsevier. All rights reserved. This content is excluded from our Creative Commons license. For more information, see <http://ocw.mit.edu/fairuse>.

- Replace integrator input resistors with 2-quadrant multipliers (voltage-controlled amplifiers, or VCA's)
 - Need to tune both VCA's together
 - Results in a wide-range tunable filter!
 - Multiplier can be used to tune Q as well

Switched-Capacitor Tunable Filters

CMOS QUAD BILATERAL SWITCH

4016



This circuit contains four independent switches that may be used for off-on control of digital or analog signals. Signals to be controlled must be less than +5 and more than -5 volts.

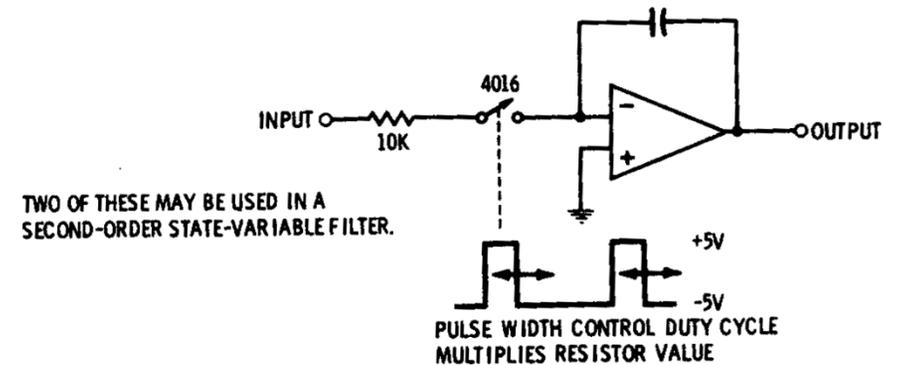
+5 volts applied to pin 13 turns ON the connection between pins 1 and 2. -5 volts applied to pin 13 turns OFF the connection between pins 1 and 2. The other three switches are similarly controlled.

Input impedance to pin 13 is essentially an open circuit. The OFF resistance of pins 1 and 2 is many megohms; the ON resistance is 300 ohms. A lower-impedance, improved version is available as the 4066.

© Elsevier Science and Technology. All rights reserved. This content is excluded from our Creative Commons license. For more information, see <http://ocw.mit.edu/fairuse>.

Many types of analog switches are available (e.g., ADG from Analog Devices, etc.)

(B) Selecting resistors under digital command (D/A conversion).



TWO OF THESE MAY BE USED IN A
SECOND-ORDER STATE-VARIABLE FILTER.

(C) Duty-cycle modulator provides variable resistance. Switching rate must be much faster than signal frequencies.

Fig. 9-7. Using the 4016 switch.

© Elsevier Science and Technology. All rights reserved. This content is excluded from our Creative Commons license. For more information, see <http://ocw.mit.edu/fairuse>.

- R is effectively varied proportionally to the On/Off duty cycle
 - Beware of aliasing (max input frequency is under half the switching frequency)
 - Not for High Pass filters!
- Tend to work best for lower-frequencies

Filters from Hong

Linear has come out with a couple really nice switched cap filters that really cuts down on the design time:

LTC1564 Tunable low pass filter 10kHz to 150kHz in steps of 10kHz, 8 pole roll-off, programmable 1-16 gain, 3-10V operation.

LTC1062 parallel 5-pole tunable low pass filter. Absolutely zero DC error because the input and output are connected directly with a wire and the filter damps out the high frequencies.

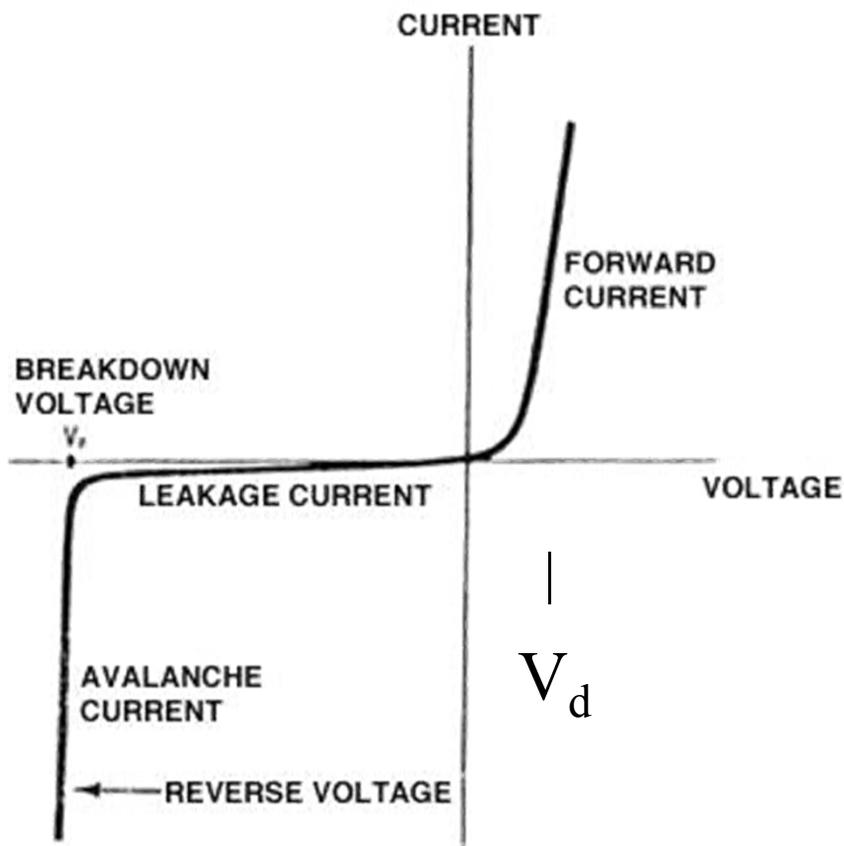


Biassing

- AC Coupling
- Biassing noninverting input
- Biassing at inverting input

Diodes

- The Diode
 - I/V characteristic, ideal diode, forward drop, zeners



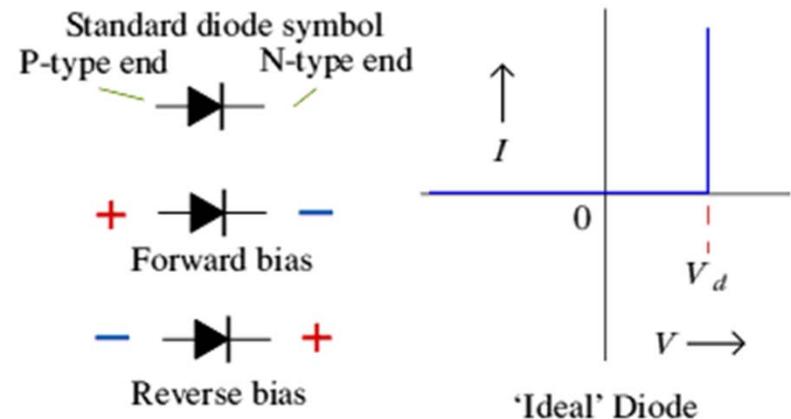
Drops (V_d):

Si = 0.6 V

Ge = 0.3 V

LED = 2.4-3.5 V

Schottky = .1-.3 V



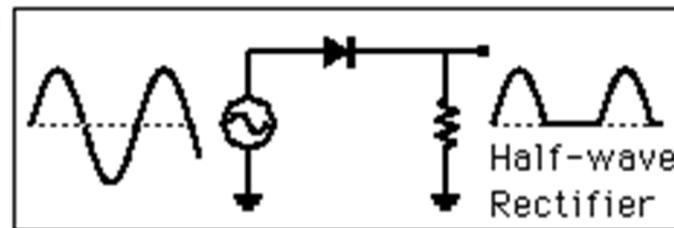
© Unknown. All rights reserved. This content is excluded from our Creative Commons license. For more information, see <http://ocw.mit.edu/fairuse>.

Basic Diode Circuits

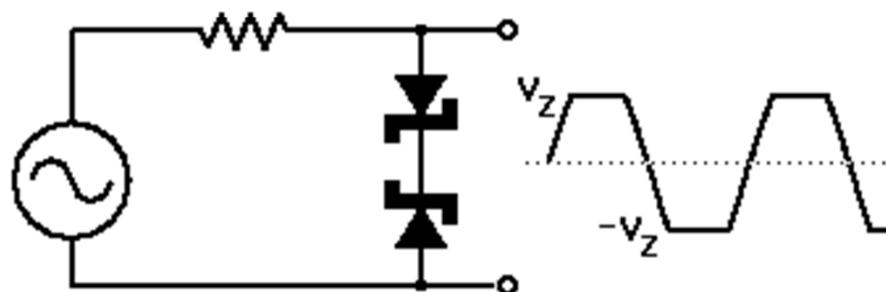
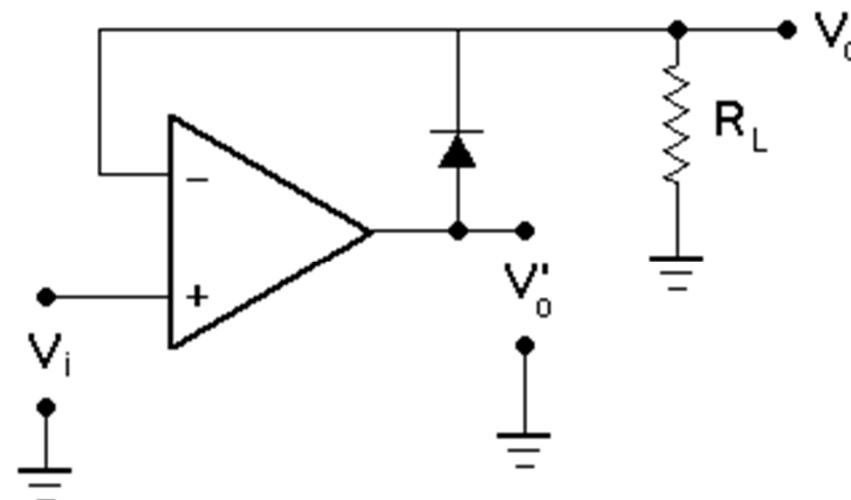
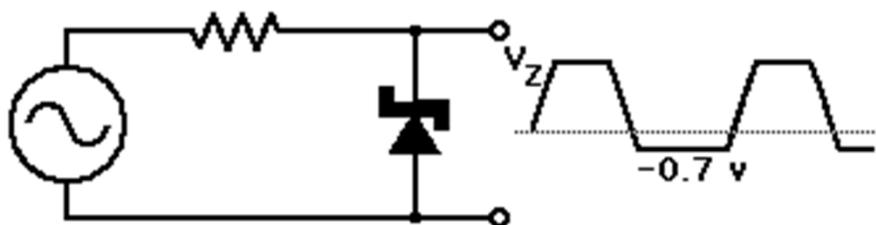
• Limiters/Clampers

– Passive Limiter - normal and zener

– Precision Zener



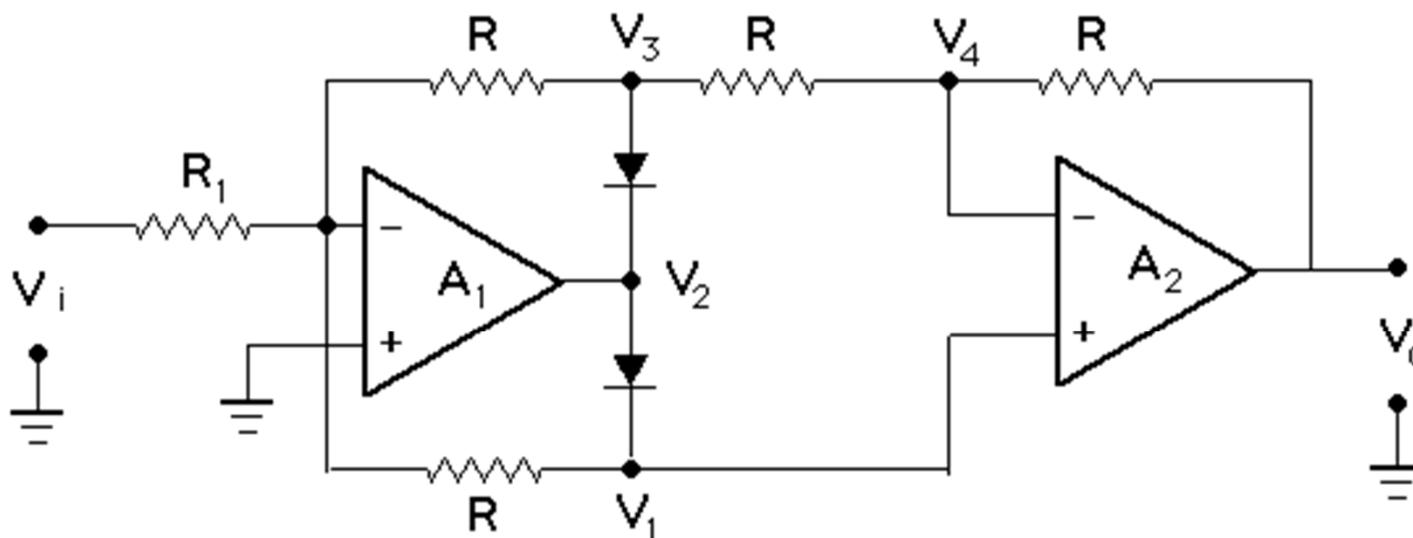
Positive Clamper



Zener Limiters

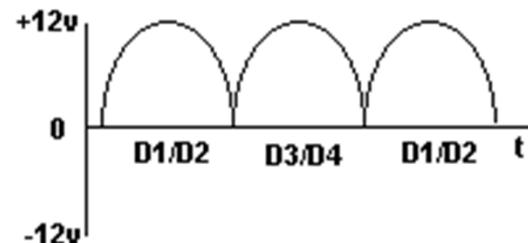
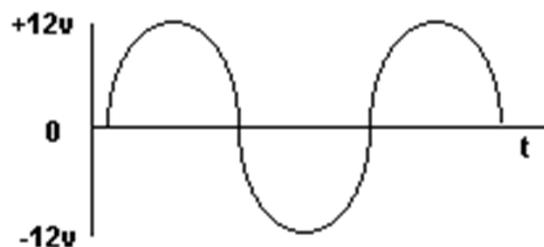
© Unknown. All rights reserved. This content is excluded from our Creative Commons license. For more information, see <http://ocw.mit.edu/fairuse>.

Absolute Value Circuits



Full Wave Rectifier Circuit

© Unknown. All rights reserved. This content is excluded from our Creative Commons license. For more information, see <http://ocw.mit.edu/fairuse>.



Bottom R is 2/3 top R in A₁?

© Unknown. All rights reserved. This content is excluded from our Creative Commons license. For more information, see <http://ocw.mit.edu/fairuse>.

Absolute Value Circuit (envelope follower)

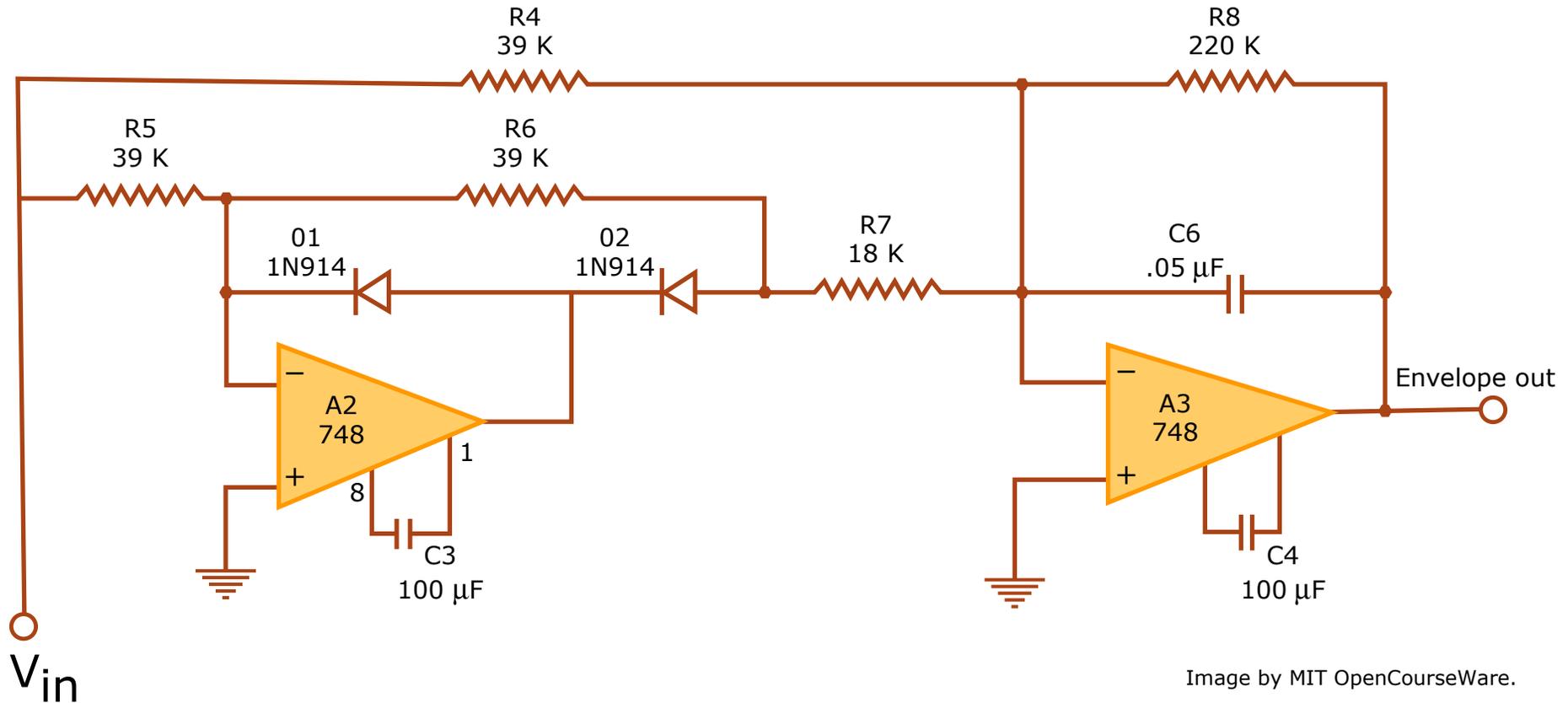
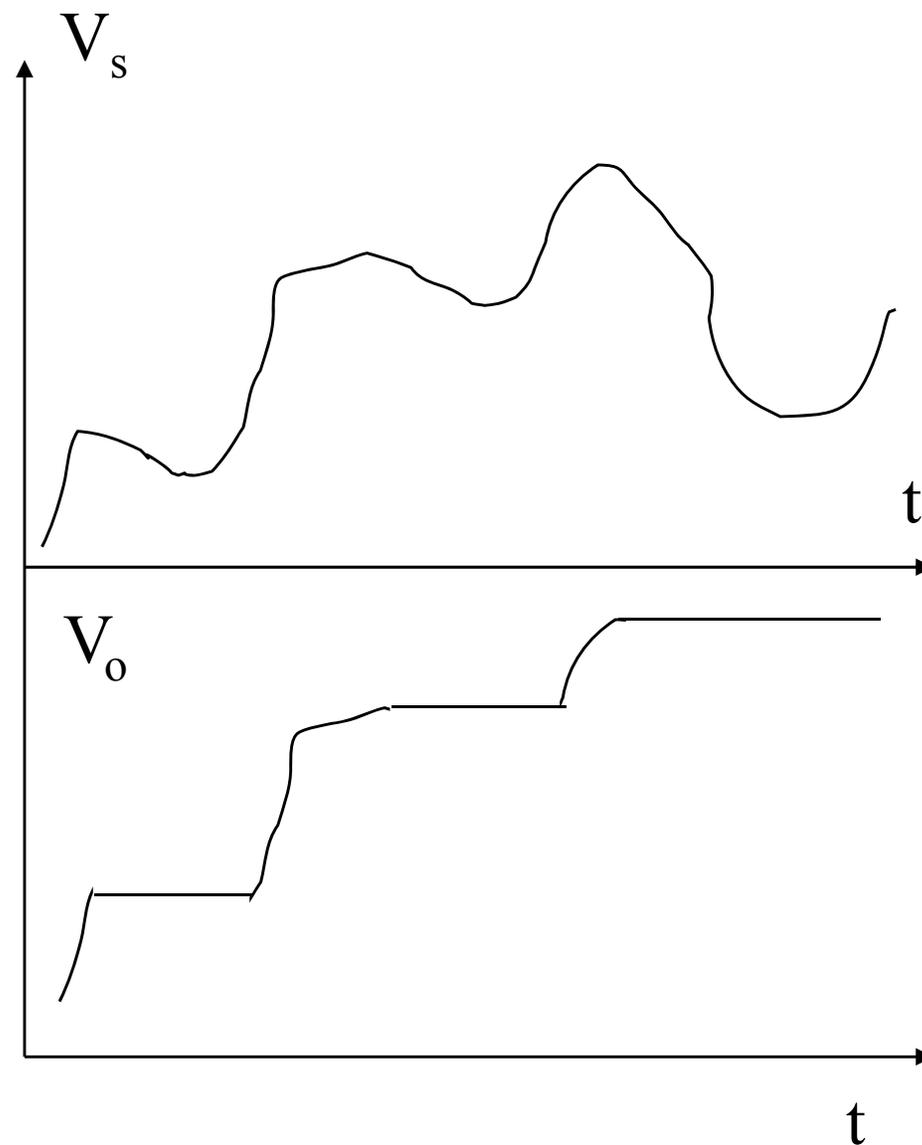
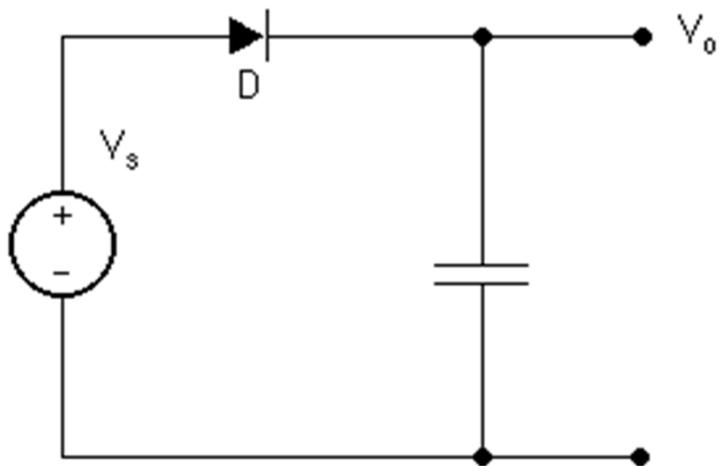


Image by MIT OpenCourseWare.

- A1 and A2 form an absolute value detector
- C6 integrates the absolute value to give the envelope
- Note that the 748 (and its compensation cap) is long obsolete!

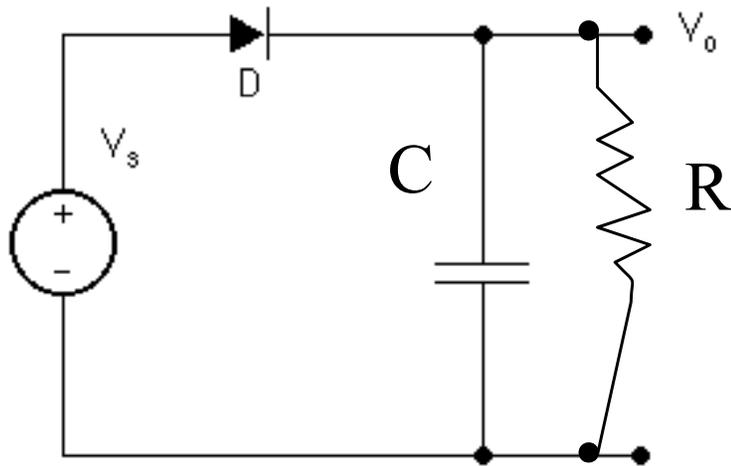
Peak Detector



Capacitor holds peaks!

Need reset switch to continue tracking

Pulse Stretcher

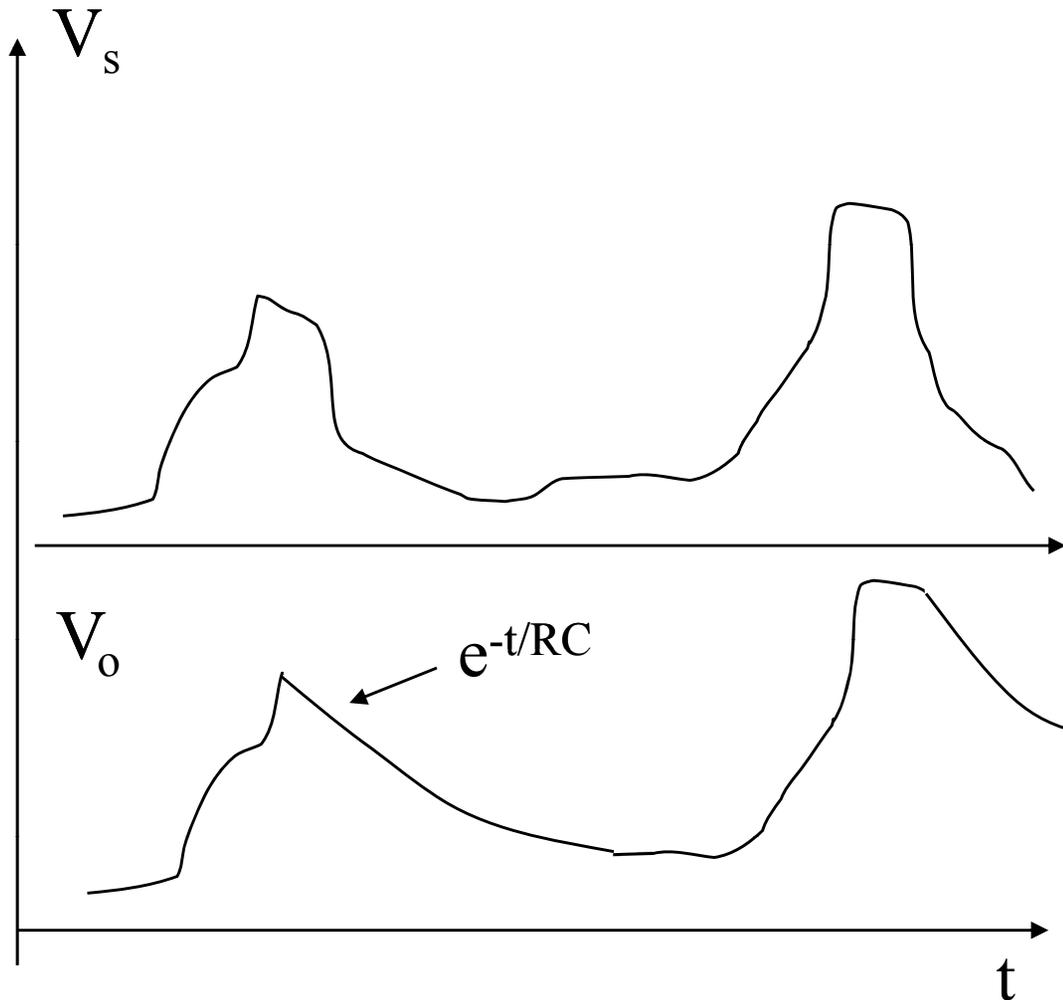


-Resistor continually (and slowly) bleeds capacitor charge

-Automatic “reset”

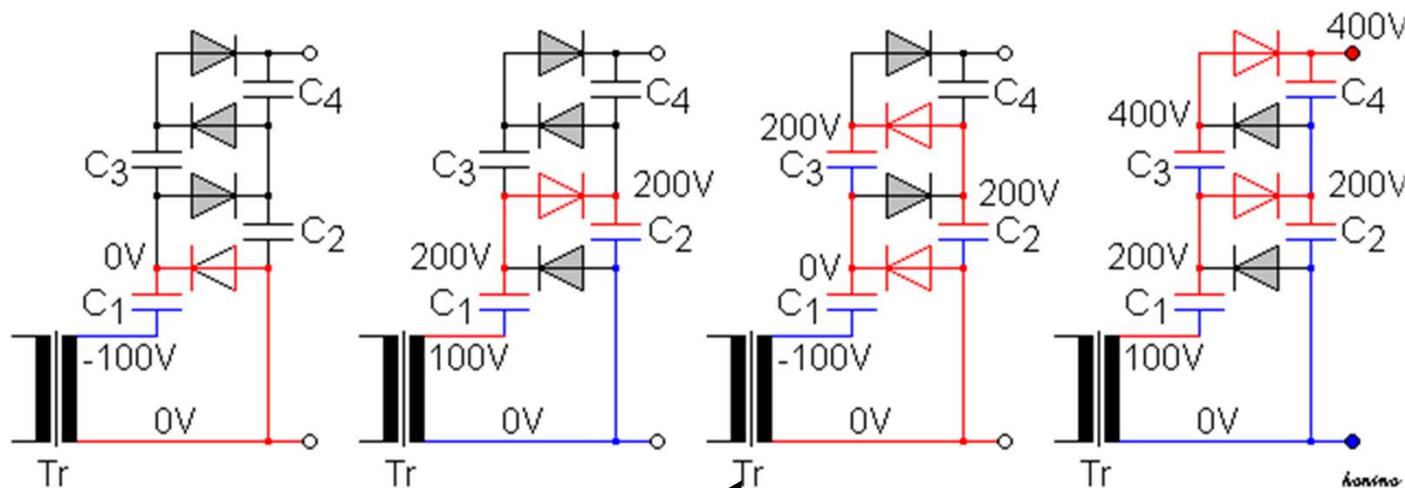
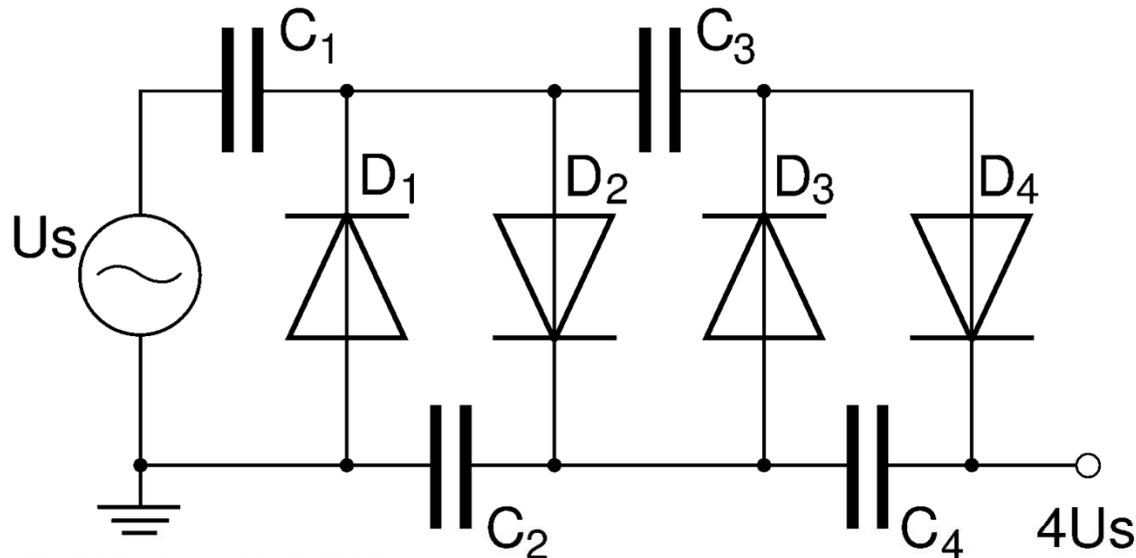
-Tune time constant to match signal dynamics (so peaks are always followed)

-Enables “lazy” sampling to catch transients



Voltage Multipliers, etc.

Cascaded Villard doubler



Ref: Wikipedia...

Transformer for isolation

- Diodes don't let capacitors discharge onto source
- AC coupling lets each peak sit atop capacitor voltage
- Each AC peak increments voltage by half-wave height
- Voltage drop at given current increases rapidly (cube) with no. stages, inversely with C , freq

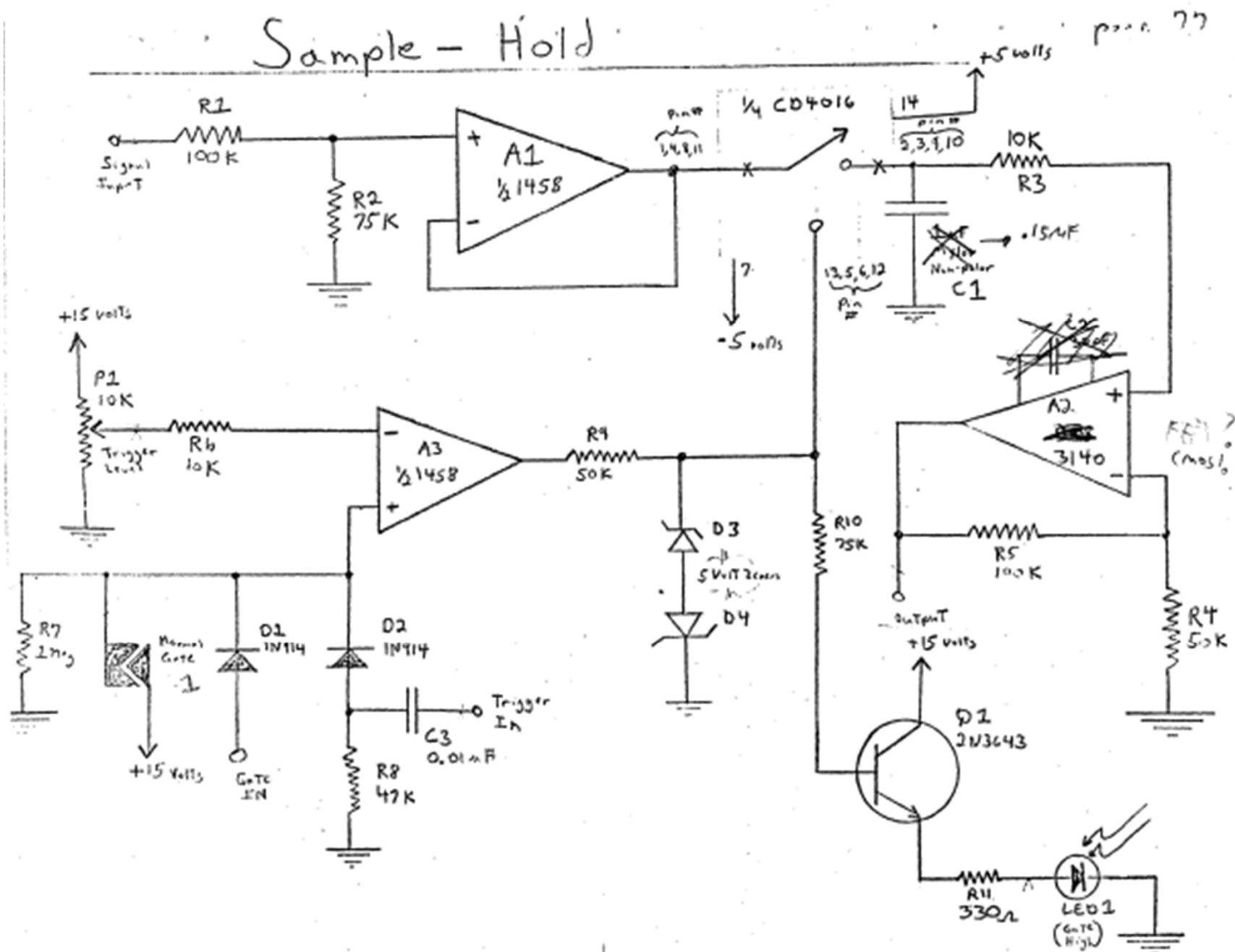
Sampling

- Nyquist: $f_{\text{in}} < f_s/2$
- Bandlimited (demodulation) sampling
 - $\Delta f_{\text{in}} < f_s/2$
 - Loose absolute phase information
 - Don't know whether phase moves forward or backward
 - Quadrature sampling
 - Bandlimited sampling at t and a quarter-period later

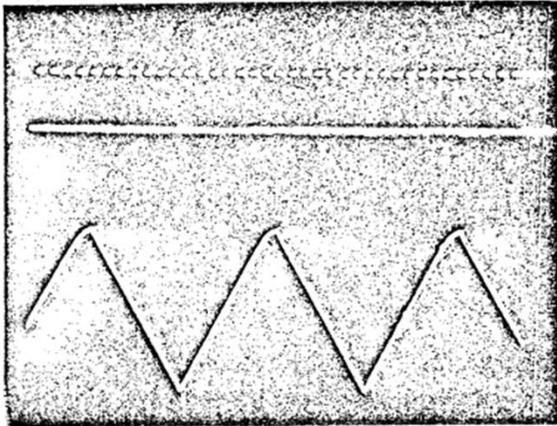
Sampling Aids

- Aliasing for nonperiodic signals??
 - Can miss or miss-sample transients!
 - The Pulse-stretcher to the rescue!
- Sample/Holds
- Analog Multiplexers
- Programmable Gain Amplifiers (PGA's)
- Voltage-Controlled Amplifiers (VCA's)

The Basic Sample-Hold Circuit



The Sample-Hold (and Track-Hold)

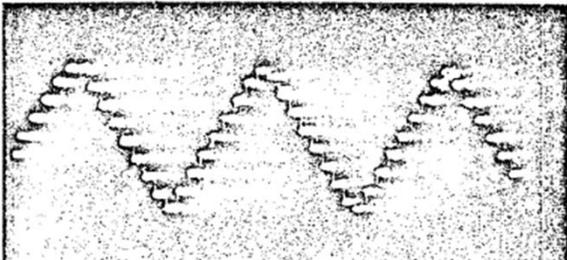


Pulse input to trigger
on S/H

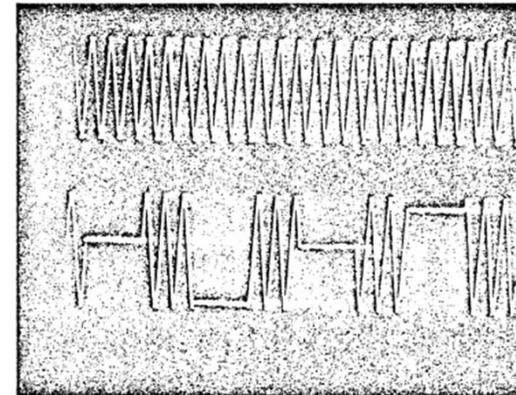
Triangle wave at the
sampled input of S/H



Part B:
Square wave applied to
the gate input of S/H
to yield photo#27



Part A:
Output of S/H when
waveforms in photo#25
are input



Waveform at S/H's
sample input

Output of S/H with
above wave at input
and the square wave in
Part B of Photo#26 at
the gate input

© Unknown. All rights reserved. This content is excluded from our Creative Commons license. For more information, see <http://ocw.mit.edu/fairuse>.

- Sample-Hold grabs input signal and holds it upon receipt of a pulse edge
- Track-Hold follows the input signal when the gate is high, but holds (latches) it when the gate is low.
- Sample hold acquires quickly – can use slow ADC.

Analog Multiplexers



CMOS
4-/8-Channel Analog Multiplexers

AD7501/AD7502/AD7503

FEATURES

DTL/TTL/CMOS Direct Interface
Power Dissipation: 30 μ W
 R_{on} : 170 Ω
Standard 16-Lead DIPs and 20-Terminal Surface Mount Packages

GENERAL DESCRIPTION

The AD7501 and AD7503 are monolithic CMOS, 8-channel analog multiplexers which switch one of eight inputs to a common output, depending on the state of three binary address lines and an "enable" input. The AD7503 is identical to the AD7501 except its "enable" logic is inverted. All digital inputs are TTL/DTL and CMOS logic compatible.

The AD7502 is a monolithic CMOS dual 4-channel analog multiplexer. Depending on the state of two binary address inputs and an "enable," it switches two output buses to two of eight inputs.

Truth Tables

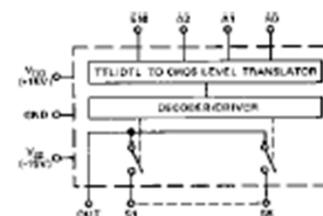
AD7501

A_2	A_1	A_0	EN	"ON"
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8
X	X	X	0	None

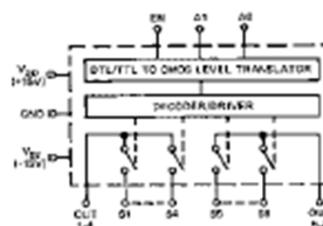
AD7503

A_2	A_1	A_0	EN	"ON"
0	0	0	0	1
0	0	1	0	2
0	1	0	0	3
0	1	1	0	4
1	0	0	0	5
1	0	1	0	6
1	1	0	0	7
1	1	1	0	8
X	X	X	1	None

FUNCTIONAL BLOCK DIAGRAM
AD7501/AD7503



AD7502

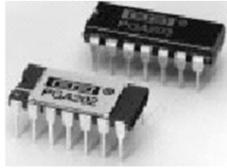


AD7502

A_1	A_0	EN	"ON"
0	0	1	1 & 5
0	1	1	2 & 6
1	0	1	3 & 7
1	1	1	4 & 8
X	X	0	None

Programmable Gain Amplifiers

BURR-BROWN®
BB



PGA202/203

BURR-BROWN®
BB



PGA206
PGA207

Digitally Controlled Programmable-Gain INSTRUMENTATION AMPLIFIER

FEATURES

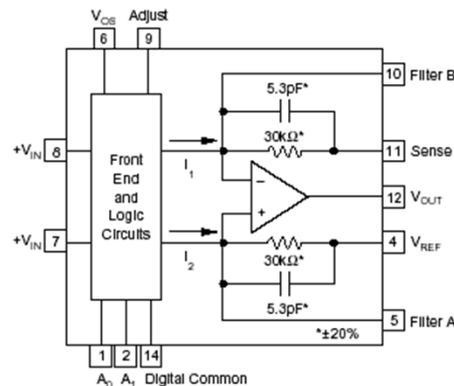
- DIGITALLY PROGRAMMABLE GAINS:
DECADE MODEL—PGA202
GAINS OF 1, 10, 100, 1000
BINARY MODEL—PGA203
GAINS OF 1, 2, 4, 8
- LOW BIAS CURRENT: 50pA max
- FAST SETTLING: 2 μ s to 0.01%
- LOW NON-LINEARITY: 0.012% max
- HIGH CMRR: 80dB min
- NEW TRANSCONDUCTANCE CIRCUITRY
- LOW COST

APPLICATIONS

- DATA ACQUISITION SYSTEMS
- AUTO-RANGING CIRCUITS
- DYNAMIC RANGE EXPANSION
- REMOTE INSTRUMENTATION
- TEST EQUIPMENT

DESCRIPTION

The PGA202 is a monolithic instrumentation amplifier with digitally controlled gains of 1, 10, 100, and 1000. The PGA203 provides gains of 1, 2, 4, and 8. Both have TTL or CMOS-compatible inputs for easy microprocessor interface. Both have FET inputs and a new transconductance circuitry that keeps the bandwidth nearly constant with gain. Gain and offsets are laser trimmed to allow use without any external components. Both amplifiers are available in ceramic or plastic packages. The ceramic package is specified over the full industrial temperature range while the plastic package covers the commercial range.



High-Speed Programmable Gain INSTRUMENTATION AMPLIFIER

FEATURES

- DIGITALLY PROGRAMMABLE GAINS:
PGA206: G=1, 2, 4, 8V/V
PGA207: G=1, 2, 5, 10V/V
- TRUE INSTRUMENTATION AMP INPUT
- FAST SETTLING: 3.5 μ s to 0.01%
- FET INPUT: $I_B = 100$ pA max
- INPUT PROTECTION: ± 40 V
- LOW OFFSET VOLTAGE: 1.5mV max
- 16-PIN DIP, SOL-16 SOIC PACKAGES

DESCRIPTION

The PGA206 and PGA207 are digitally programmable gain instrumentation amplifiers that are ideally suited for data acquisition systems.

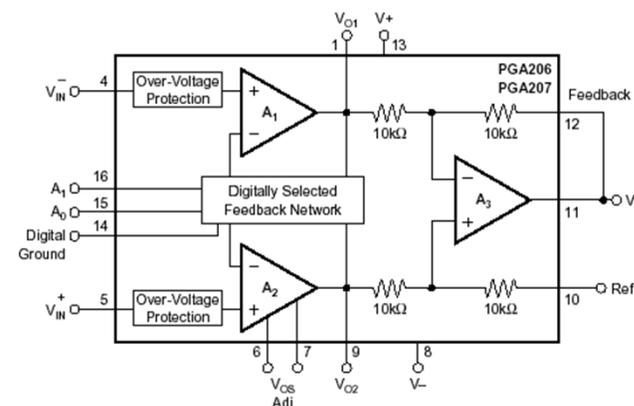
The PGA206 and PGA207's fast settling time allows multiplexed input channels for excellent system efficiency. FET inputs eliminate I_B errors due to analog multiplexer series resistance.

Gains are selected by two CMOS/TTL-compatible address lines. Analog inputs are internally protected for overloads up to ± 40 V, even with the power supplies off. The PGA206 and PGA207 are laser-trimmed for low offset voltage and low drift.

The PGA206 and PGA207 are available in 16-pin plastic DIP and SOL-16 surface-mount packages. Both are specified for -40°C to $+85^\circ\text{C}$ operation.

APPLICATIONS

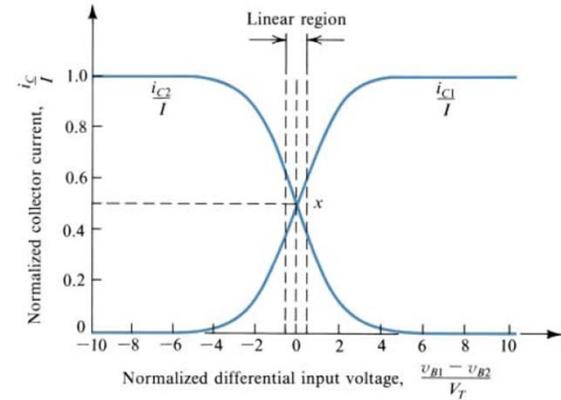
- MULTIPLE-CHANNEL DATA ACQUISITION
- MEDICAL, PHYSIOLOGICAL AMPLIFIER
- PC-CONTROLLED ANALOG INPUT BOARDS



Front end of the OTA

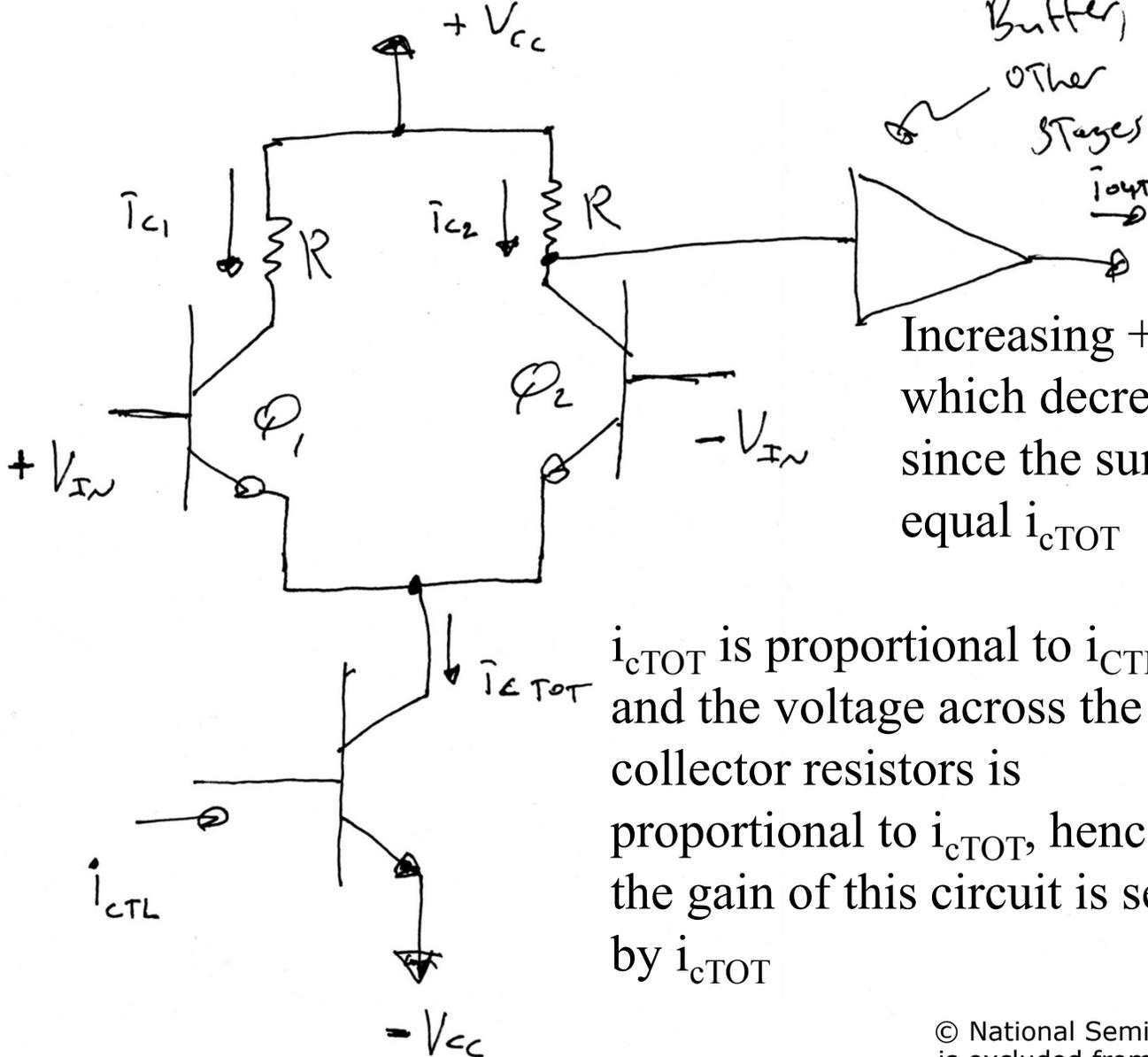
$$I_{ctot} = i_{c1} + i_{c2} = \beta i_{CTL}$$

OTAs have
current outputs



MTU ECE Diff Amp Notes

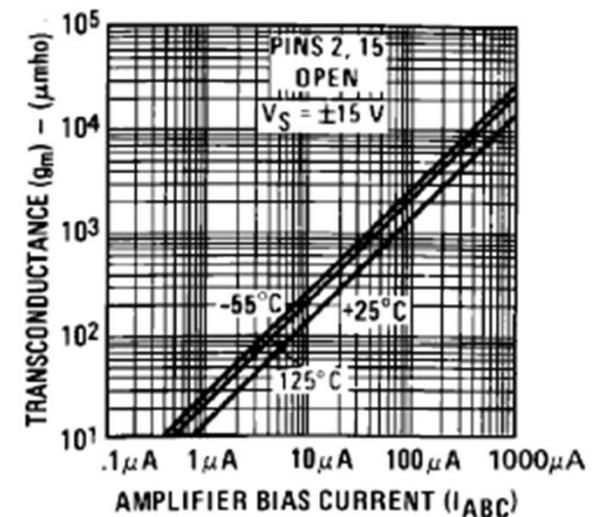
© Unknown. All rights reserved. This content is excluded from our Creative Commons license. For more information, see <http://ocw.mit.edu/fairuse>.



Increasing $+V_{IN}$ increases i_{c1} ,
which decreases i_{c2} (for fixed $-V_{IN}$)
since the sum of i_{c1} and i_{c2} must
equal i_{cTOT}

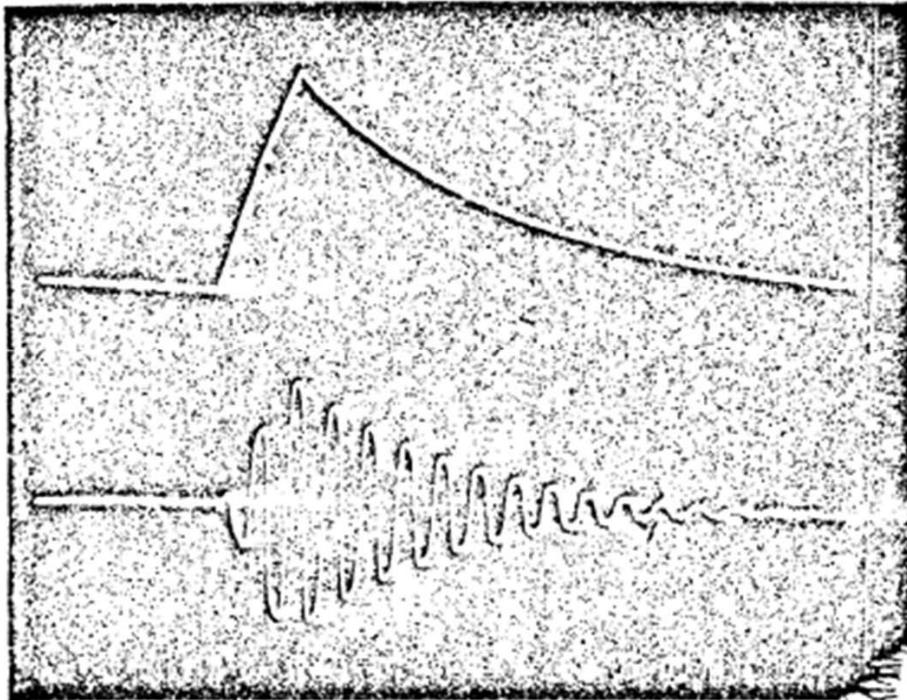
i_{cTOT} is proportional to i_{CTL} ,
and the voltage across the
collector resistors is
proportional to i_{cTOT} , hence
the gain of this circuit is set
by i_{cTOT}

LM13700 Datasheet



© National Semiconductor. All rights reserved. This content is excluded from our Creative Commons license. For more information, see <http://ocw.mit.edu/fairuse>.

Voltage Controlled Amplifiers



© Unknown. All rights reserved. This content is excluded from our Creative Commons license. For more information, see <http://ocw.mit.edu/fairuse>.

VCA output for sinusoidal input and given control voltage

$$V_{\text{out}} = V_{\text{in}} * V_{\text{ctl}} \text{ (or 0 if } V_{\text{ctl}} < 0)$$

Voltage-Controlled Amplifiers (VCA)

Burr-Brown Products
from Texas Instruments

VCA610



www.ti.com

WIDEBAND VOLTAGE CONTROLLED AMPLIFIER

FEATURES

- WIDE GAIN CONTROL RANGE: 77dB
- SMALL PACKAGE: SO-8
- WIDE SIGNAL BANDWIDTH: 30MHz
- LOW VOLTAGE NOISE: $2.2\text{nV}/\sqrt{\text{Hz}}$
- FAST GAIN SLEW RATE: $300\text{dB}/\mu\text{s}$

APPLICATIONS

- OPTICAL DISTANCE MEASUREMENT
- AGC AMPLIFIERS
- ULTRASOUND
- SONAR
- ACTIVE FILTERS
- LOG AMPLIFIERS
- IF CIRCUITS
- CCD CAMERAS

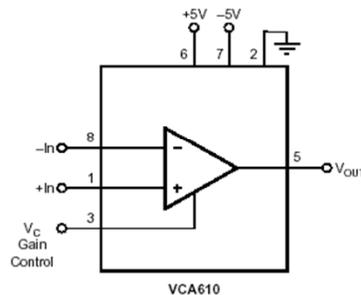
DESCRIPTION

The VCA610 is a wideband, continuously variable, voltage-controlled gain amplifier. It provides linear-dB gain control with high impedance inputs. It is designed to be used as a flexible gain-control element in a variety of electronic systems.

The VCA610 has a gain-control range of 77dB (-38.5dB to $+38.5\text{dB}$) providing both gain and attenuation for maximum flexibility in a small SO-8. The broad attenuation range can be used for gradual or controlled channel turn-on and turn-off for applications in which abrupt gain changes can create artifacts or other errors. In addition, the output can be disabled to provide -77dB of attenuation. Group delay variation with gain is typically less than $\pm 2\text{ns}$ across a bandwidth of 1MHz to 15MHz.

The VCA610 has a noise figure of 3.5dB (with an R_g of 200Ω) including the effects of both current and voltage noise. Instantaneous output dynamic range is 70dB for gains of 0dB to $+38.5\text{dB}$ with 1MHz noise bandwidth. The output is capable of driving 100Ω . The high-speed, $300\text{dB}/\mu\text{s}$, gain-control signal is a unipolar (0V to -2V) voltage that varies the gain linearly in dB/V over a -38.5dB to $+38.5\text{dB}$ range.

The VCA610 is designed with a very fast overload recovery time of only 200ns. This allows a large signal transient to overload the output at high gain, without obscuring low-level signals following closely behind. The excellent overload recovery time and distortion specifications optimize this device for low-level doppler measurements.



**TEXAS
INSTRUMENTS**

**ANALOG
DEVICES**

Dual, Low Noise, Wideband Variable Gain Amplifiers

AD600/AD602*

FEATURES

Two Channels with Independent Gain Control
"Linear in dB" Gain Response

Two Gain Ranges:

AD600: 0 dB to 40 dB

AD602: -10 dB to $+30\text{ dB}$

Accurate Absolute Gain: $\pm 0.3\text{ dB}$

Low Input Noise: $1.4\text{ nV}/\sqrt{\text{Hz}}$

Low Distortion: -60 dBc THD at $\pm 1\text{ V}$ Output

High Bandwidth: DC to 35 MHz (-3 dB)

Stable Group Delay: $\pm 2\text{ ns}$

Low Power: 125 mW (Max) per Amplifier

Signal Gating Function for Each Amplifier

Drives High-Speed A/D Converters

MIL-STD-883-Compliant and DESC Versions Available

APPLICATIONS

Ultrasound and Sonar Time-Gain Control

High-Performance Audio and RF AGC Systems

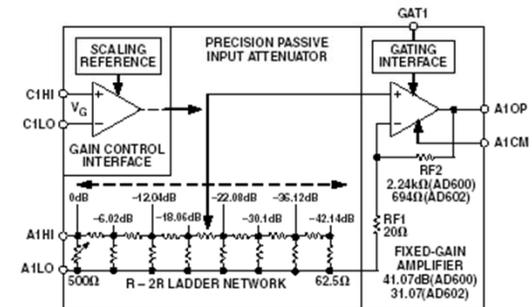
Signal Measurement

PRODUCT DESCRIPTION

The AD600 and AD602 dual channel, low noise variable gain amplifiers are optimized for use in ultrasound imaging systems, but are applicable to any application requiring very precise gain, low noise and distortion, and wide bandwidth. Each independent channel provides a gain of 0 dB to $+40\text{ dB}$ in the AD600 and -10 dB to $+30\text{ dB}$ in the AD602. The lower gain of the AD602 results in an improved signal-to-noise ratio at the output. However, both products have the same $1.4\text{ nV}/\sqrt{\text{Hz}}$ input noise spectral density. The decibel gain is directly proportional to the control voltage, is accurately calibrated, and is supply- and temperature-stable.

To achieve the difficult performance objectives, a proprietary circuit form—the X-AMP[®]—has been developed. Each channel of the X-AMP comprises a variable attenuator of 0 dB to -42.14 dB followed by a high speed fixed gain amplifier. In this way, the amplifier never has to cope with large inputs, and can benefit from the use of negative feedback to precisely define the gain and dynamics. The attenuator is realized as a seven-stage R-2R ladder network having an input resistance of 100Ω , laser-trimmed to $\pm 2\%$. The attenuation between tap points is 6.02 dB; the gain-control circuit provides continuous interpolation between these taps. The resulting control function is linear in dB.

FUNCTIONAL BLOCK DIAGRAM



The gain-control interfaces are fully differential, providing an input resistance of $\sim 15\text{ M}\Omega$ and a scale factor of 32 dB/V (that is, $31.25\text{ mV}/\text{dB}$) defined by an internal voltage reference. The response time of this interface is less than 1 μs . Each channel also has an independent gating facility that optionally blocks signal transmission and sets the dc output level to within a few millivolts of the output ground. The gating control input is TTL and CMOS compatible.

The maximum gain of the AD600 is 41.07 dB, and that of the AD602 is 31.07 dB; the -3 dB bandwidth of both models is nominally 35 MHz, essentially independent of the gain. The signal-to-noise ratio (SNR) for a 1 V rms output and a 1 MHz noise bandwidth is typically 76 dB for the AD600 and 86 dB for the AD602. The amplitude response is flat within $\pm 0.5\text{ dB}$ from 100 kHz to 10 MHz; over this frequency range the group delay varies by less than $\pm 2\text{ ns}$ at all gain settings.

Each amplifier channel can drive 100Ω load impedances with low distortion. For example, the peak specified output is $\pm 2.5\text{ V}$ minimum into a 500Ω load, or $\pm 1\text{ V}$ into a 100Ω load. For a 200Ω load in shunt with 5 pF, the total harmonic distortion for a $\pm 1\text{ V}$ sinusoidal output at 10 MHz is typically -60 dBc .

The AD600J and AD602J are specified for operation from 0°C to 70°C , and are available in both 16-lead plastic DIP (N) and 16-lead SOIC (R). The AD600A and AD602A are specified for operation from -40°C to $+85^\circ\text{C}$ and are available in both 16-lead cerdip (Q) and 16-lead SOIC (R).

The AD600S and AD602S are specified for operation from -55°C to $+125^\circ\text{C}$ and are available in a 16-lead cerdip (Q) package and are MIL-STD-883 compliant. The AD600S and AD602S are also available under DESC SMD 5962-94572.

VCA Arrays



Low Cost Quad Voltage Controlled Amplifier

SSM2164

FEATURES

Four High Performance VCAs in a Single Package
 0.02% THD
 No External Trimming
 120 dB Gain Range
 0.07 dB Gain Matching (Unity Gain)
 Class A or AB Operation

APPLICATIONS

Remote, Automatic, or Computer Volume Controls
 Automotive Volume/Balance/Faders
 Audio Mixers
 Compressor/Limiters/Compondors
 Noise Reduction Systems
 Automatic Gain Controls
 Voltage Controlled Filters
 Spatial Sound Processors
 Effects Processors

GENERAL DESCRIPTION

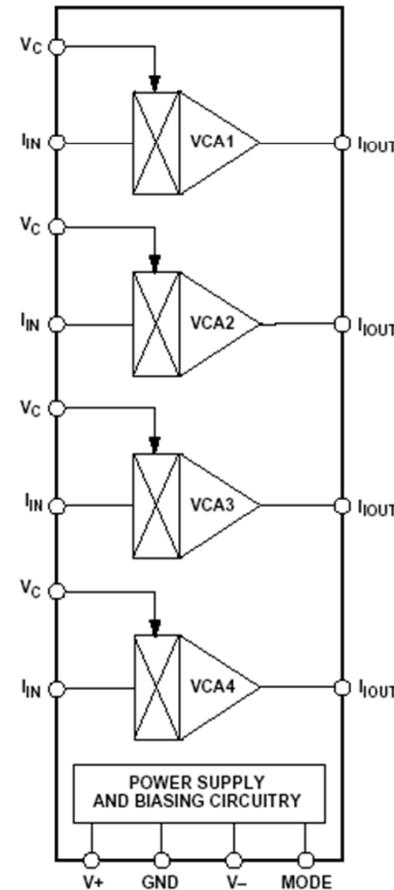
The SSM2164 contains four independent voltage controlled amplifiers (VCAs) in a single package. High performance (100 dB dynamic range, 0.02% THD) is provided at a very low cost-per-VCA, resulting in excellent value for cost sensitive gain control applications. Each VCA offers current input and output for maximum design flexibility, and a ground referenced -33 mV/dB control port.

All channels are closely matched to within 0.07 dB at unity gain, and 0.24 dB at 40 dB of attenuation. A 120 dB gain range is possible.

A single resistor tailors operation between full Class A and AB modes. The pinout allows upgrading of SSM2024 designs with minimal additional circuitry.

The SSM2164 will operate over a wide supply voltage range of ± 4 V to ± 18 V. Available in 16-pin P-DIP and SOIC packages, the device is guaranteed for operation over the extended industrial temperature range of -40°C to $+85^{\circ}\text{C}$.

FUNCTIONAL BLOCK DIAGRAM



Analog Multipliers (4-Quadrant)



Low Cost
Analog Multiplier

AD633

FEATURES

4-Quadrant Multiplication
Low Cost 8-Lead Package
Complete—No External Components Required
Laser-Trimmed Accuracy and Stability
Total Error within 2% of FS
Differential High Impedance X and Y Inputs
High Impedance Unity-Gain Summing Input
Laser-Trimmed 10 V Scaling Reference

APPLICATIONS

Multiplication, Division, Squaring
Modulation/Demodulation, Phase Detection
Voltage Controlled Amplifiers/Attenuators/Filters

4 Quadrant means:
Multiplying by
negative values
(negative voltages)
inverts the output.
Either input can go
negative.

VCA's are 2 Quadrant
devices – the control
input can't go
negative, although the
signal input can.

PRODUCT DESCRIPTION

The AD633 is a functionally complete, four-quadrant, analog multiplier. It includes high impedance, differential X and Y inputs and a high impedance summing input (Z). The low impedance output voltage is a nominal 10 V full scale provided by a buried Zener. The AD633 is the first product to offer these features in modestly priced 8-lead plastic DIP and SOIC packages.

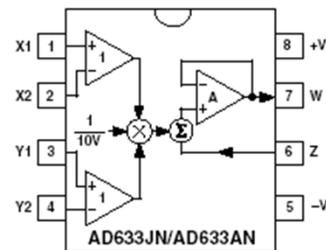
The AD633 is laser calibrated to a guaranteed total accuracy of 2% of full scale. Nonlinearity for the Y input is typically less than 0.1% and noise referred to the output is typically less than 100 μV rms in a 10 Hz to 10 kHz bandwidth. A 1 MHz bandwidth, 20 V/ μs slew rate, and the ability to drive capacitive loads make the AD633 useful in a wide variety of applications where simplicity and cost are key concerns.

The AD633's versatility is not compromised by its simplicity. The Z-input provides access to the output buffer amplifier, enabling the user to sum the outputs of two or more multipliers, increase the multiplier gain, convert the output voltage to a current, and configure a variety of applications.

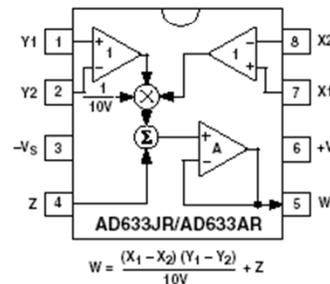
The AD633 is available in an 8-lead plastic DIP package (N) and 8-lead SOIC (R). It is specified to operate over the 0°C to 70°C commercial temperature range (J Grade) or the -40°C to +85°C industrial temperature range (A Grade).

CONNECTION DIAGRAMS

8-Lead Plastic DIP (N) Package



8-Lead Plastic SOIC (RN-8) Package



PRODUCT HIGHLIGHTS

1. The AD633 is a complete four-quadrant multiplier offered in low cost 8-lead plastic packages. The result is a product that is cost effective and easy to apply.
2. No external components or expensive user calibration are required to apply the AD633.
3. Monolithic construction and laser calibration make the device stable and reliable.
4. High (10 M Ω) input resistances make signal source loading negligible.
5. Power supply voltages can range from ± 8 V to ± 18 V. The internal scaling voltage is generated by a stable Zener diode; multiplier accuracy is essentially supply insensitive.

MIT OpenCourseWare
<http://ocw.mit.edu>

MAS.836 Sensor Technologies for Interactive Environments
Spring 2011

For information about citing these materials or our Terms of Use, visit: <http://ocw.mit.edu/terms>.